# **Small Signal MOSFET**

## 30 V, 250 mA, Dual N-Channel, SC-88

#### **Features**

- Low Gate Charge for Fast Switching
- Small Footprint 30% Smaller than TSOP-6
- ESD Protected Gate
- AEC O101 Oualified NVTJD4001N
- These Devices are Pb-Free and are RoHS Compliant

#### **Applications**

- Low Side Load Switch
- Li-Ion Battery Supplied Devices Cell Phones, PDAs, DSC
- Buck Converters
- Level Shifts

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			$V_{DSS}$	30	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain	Steady State	T <sub>A</sub> = 25 °C	I <sub>D</sub>	250	mA
Current (Note 1)		T <sub>A</sub> = 85 °C		180	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25 °C	P <sub>D</sub>	272	mW
Pulsed Drain Current t =10 μs			I <sub>DM</sub>	600	mA
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C
Source Current (Body Diode)			Is	250	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

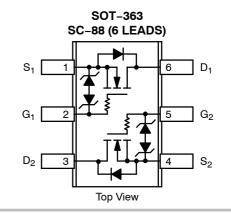
1. Surface mounted on FR4 board using min pad size (Cu area = 0.155 in sq [1 oz] including traces).



## ON Semiconductor®

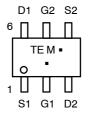
#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> Max
30 V	1.0 Ω @ 4.0 V	250 mA
	1.5 Ω @ 2.5 V	250 MA



## **MARKING DIAGRAM & PIN ASSIGNMENT**





TE = Device Code = Date Code М = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTJD4001NT1G	SOT-363 (Pb-Free)	3000 / Tape & Reel
NVTJD4001NT1G	SOT-363 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

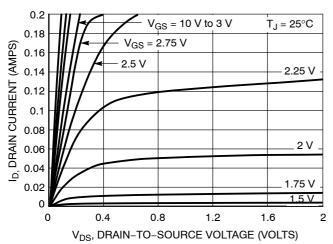
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## FI FCTRICAL CHARACTERISTICS (T = 25°C unless otherwise stated)

Parameter	Symbol	Test Cond	dition	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 100 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				56		mV/ °C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>E</sub>	<sub>OS</sub> = 30 V			1.0	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{G}$	<sub>S</sub> = ±10 V			±1.0	μΑ
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D}$	= 100 μΑ	0.8	1.2	1.5	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-3.2		mV/ °C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 10 mA			1.0	1.5	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 10 mA			1.5	2.5	
Forward Transconductance	9 <sub>FS</sub>	$V_{DS} = 3.0 \text{ V}, I_{D} = 10 \text{ mA}$			80		mS
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 5.0 \text{ V}$			20	33	pF
Output Capacitance	C <sub>OSS</sub>				19	32	
Reverse Transfer Capacitance	C <sub>RSS</sub>				7.25	12	
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = 5.0 \text{ V}, V_{DS} = 24 \text{ V},$ $I_{D} = 0.1 \text{ A}$			0.9	1.3	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				0.2		
Gate-to-Source Charge	$Q_{GS}$				0.3		
Gate-to-Drain Charge	$Q_{GD}$				0.2		
SWITCHING CHARACTERISTICS (No	ote 3)						
Turn-On Delay Time	td <sub>(ON)</sub>	$V_{GS} = 4.5 \text{ V}, V_{E}$	<sub>DD</sub> = 5.0 V,		17		ns
Rise Time	tr	$I_D$ = 10 mA, $R_G$ = 50 $Ω$			23		
Turn-Off Delay Time	td <sub>(OFF)</sub>				94		
Fall Time	tf				82		
DRAIN-SOURCE DIODE CHARACTE	RISTICS		<u> </u>				
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.65	0.7	V
		I <sub>S</sub> = 10 mA	T <sub>J</sub> = 125°C		0.45		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 8.0 \text{ A/}\mu\text{s,} \\ I_{S} = 10 \text{ mA}$			12.4		ns
		1	l l				

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

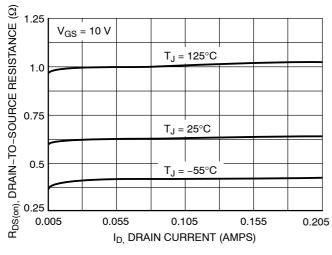
## TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)



0.1 V<sub>DS</sub> = 5 V 0.08 V<sub>DS</sub> = 5 V T<sub>J</sub> = 125°C 1.2 1.4 1.6 1.8 2 2.2 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



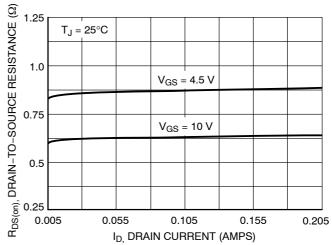
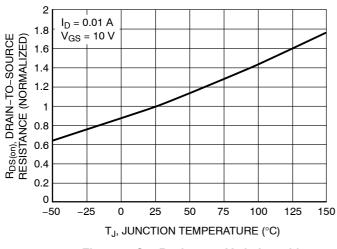


Figure 3. On-Resistance vs. Drain Current and Temperature

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



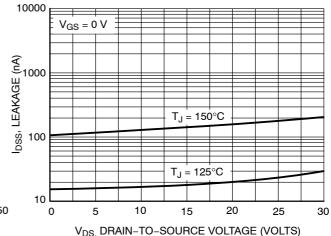
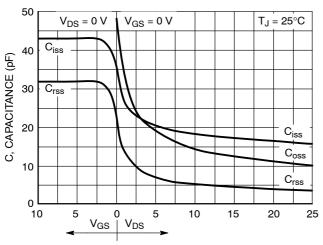
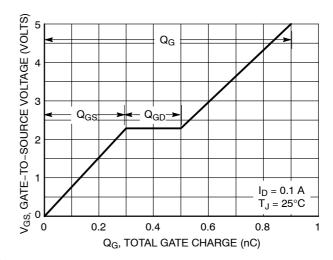


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)





GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

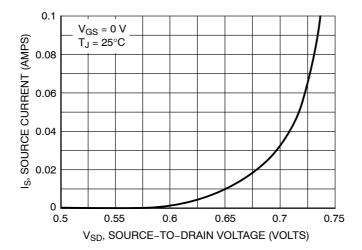


Figure 9. Diode Forward Voltage vs. Current

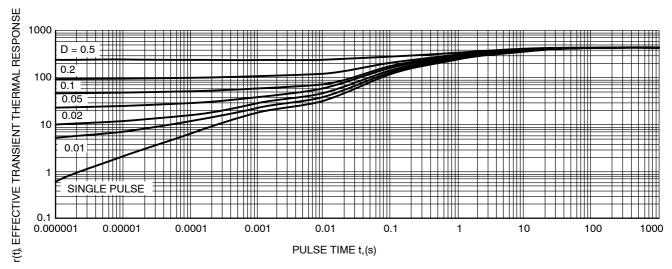
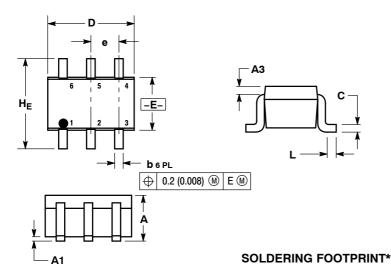


Figure 10. Thermal Response

#### PACKAGE DIMENSIONS

### SC-88/SC70-6/SOT-363 CASE 419B-02 **ISSUE W**



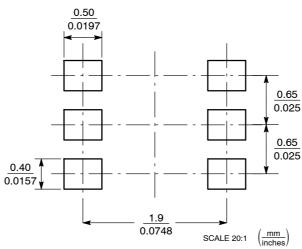
#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

	MIL	LIMETE	ERS	INCHES				
DIN	MIN	NOM	MAX	MIN	NOM	MAX		
Α	0.80	0.95	1.10	0.031	0.037	0.043		
A1	0.00	0.05	0.10	0.000	0.002	0.004		
АЗ	0.20 REF			0.008 REF				
b	0.10	0.21	0.30	0.004	0.008	0.012		
С	0.10	0.14	0.25	0.004	0.005	0.010		
D	1.80	2.00	2.20	0.070	0.078	0.086		
Е	1.15	1.25	1.35	0.045 0.049		0.053		
е		0.65 BSC			0.026 BSC			
L	0.10	0.20	0.30	0.004	0.008	0.012		
HE	2.00	2.10	2.20	0.078	0.082	0.086		

STYLE 26: PIN 1. SOURCE 1

- 2. GATE 1 3. DRAIN 2
- SOURCE 2 GATE 2
- 5. GATE 2 6. DRAIN 1



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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