BSS63LT1G, NSVBSS63LT1G

High Voltage Transistor

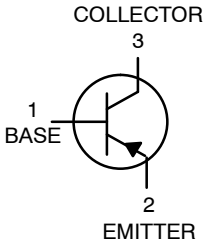
PNP Silicon

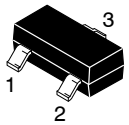
ON Semiconductor®

http://onsemi.com

Features

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable





SOT−23
CASE 318
STYLE 6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	−100	Vdc
Collector − Emitter Voltage R_{BE} = 10 kΩ	V_{CER}	−110	Vdc
Collector Current − Continuous	I_C	−100	mAdc

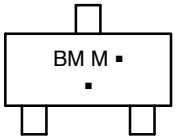
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

MARKING DIAGRAM



BM = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
BSS63LT1G	SOT−23 (Pb−free)	3000 / Tape & Reel
NSVBSS63LT1G	SOT−23 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

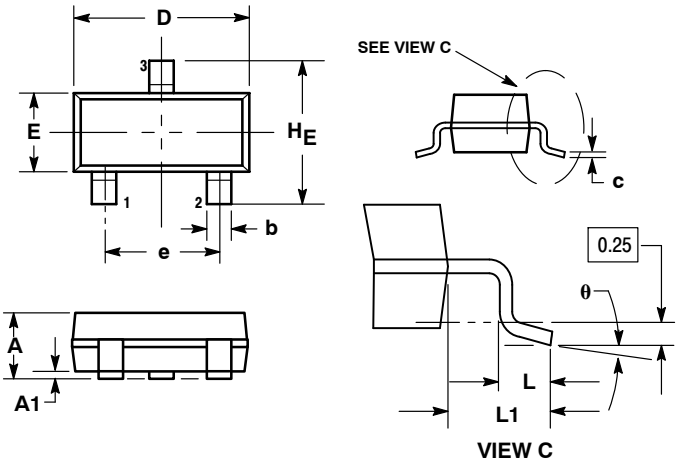
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = −100 μAdc)	$V_{(BR)CEO}$	−100	–	–	Vdc
Collector – Emitter Breakdown Voltage (I_C = −10 μAdc, I_E = 0, R_{BE} = 10 kΩ)	$V_{(BR)CER}$	−110	–	–	Vdc
Collector – Base Breakdown Voltage (I_E = −10 μAdc, I_E = 0)	$V_{(BR)CBO}$	−110	–	–	Vdc
Emitter – Base Breakdown Voltage (I_E = −10 μAdc)	$V_{(BR)EBO}$	−6.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = −90 Vdc, I_E = 0)	I_{CBO}	–	–	−100	nAdc
Collector Cutoff Current (V_{CE} = −110 Vdc, R_{BE} = 10 kΩ)	I_{CER}	–	–	−10	μAdc
Emitter Cutoff Current (V_{EB} = −6.0 Vdc, I_C = 0)	I_{EBO}	–	–	−200	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = −10 mAdc, V_{CE} = −1.0 Vdc) (I_C = −25 mAdc, V_{CE} = −1.0 Vdc)	h_{FE}	30 30	– –	– –	–
Collector – Emitter Saturation Voltage (I_C = −25 mAdc, I_B = −2.5 mAdc)	$V_{CE(sat)}$	–	–	−250	mVdc
Base – Emitter Saturation Voltage (I_C = −25 mAdc, I_B = −2.5 mAdc)	$V_{BE(sat)}$	–	–	−900	mVdc
SMALL−SIGNAL CHARACTERISTICS					
Current – Gain – Bandwidth Product (I_C = −25 mAdc, V_{CE} = −5.0 Vdc, f = 20 MHz)	f_T	50	95	–	MHz
Case Capacitance (I_E = I_C = 0, V_{CB} = −10 Vdc, f = 1.0 MHz)	C_C	–	–	20	pF

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

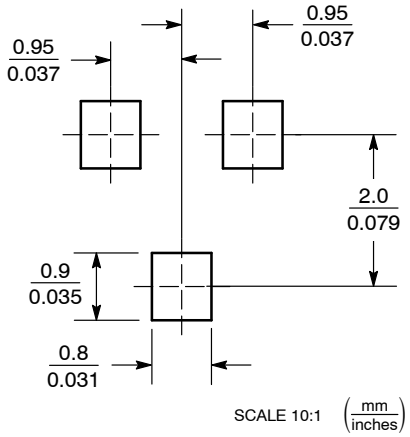


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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