



# FSA2567 — Low-Power, Dual SIM Card Analog Switch

## Features

- Low On Capacitance for Data Path: 10 pF Typical
- Low On Resistance for Data Path: 6 Ω Typical
- Low On Resistance for Supply Path: 0.4 Ω Typical
- Wide V<sub>CC</sub> Operating Range: 1.65 V to 4.3 V
- Low Power Consumption: 1 μA Maximum
  - 15 μA Maximum I<sub>CCCT</sub> Over Expanded Voltage Range (V<sub>IN</sub>=1.8 V, V<sub>CC</sub>=4.3 V)
- Wide -3 db Bandwidth: > 160 MHz
- Packaged in:
  - Pb-free 16-Lead MLP & 16-Lead UMLP
- 3 kV ESD Rating, >12 kV Power/GND ESD Rating

## Description

The FSA2567 is a bi-directional, low-power, dual double-pole, double-throw (4PDT) analog switch targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The FSA2567 is compatible with the requirements of SIM cards and features a low on capacitance (C<sub>ON</sub>) of 10 pF to ensure high-speed data transfer. The V<sub>SIM</sub> switch path has a low R<sub>ON</sub> characteristic to ensure minimal voltage drop in the dual SIM card supply paths.

The FSA2567 contains special circuitry that minimizes current consumption when the control voltage applied to the SEL pin is lower than the supply voltage (V<sub>CC</sub>). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

## Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

## Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA2567MPX	FSA2567	-40 to +85°C	16-Lead, Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3 mm Square
FSA2567UMX	GX		16-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6 mm

For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

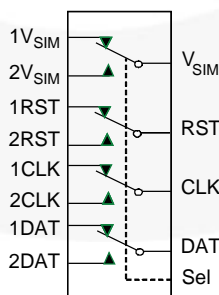
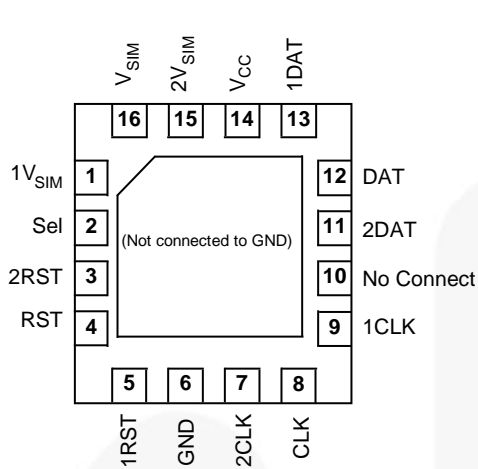
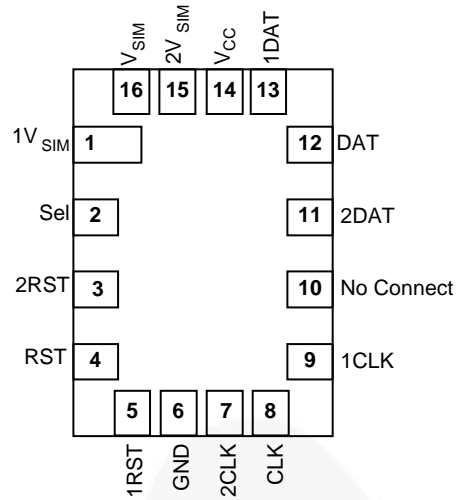


Figure 1. Analog Symbol

## Pin Assignments



**Figure 2. Pad Assignment MLP16 (Top Through View)**



**Figure 3. Pad Assignment UMLP16 (Top Through View)**

## Pin Definitions

Pin	Description
nDAT, nRST, nCLK	Multiplexed Data Source Inputs
nV <sub>SIM</sub>	Multiplexed SIM Supply Inputs
V <sub>SIM</sub> , DAT, RST, CLK	Common SIM Ports
Sel	Switch Select

## Truth Table

Sel	Function
Logic LOW	1DAT = DAT, 1RST = RST, 1CLK = CLK, 1V <sub>SIM</sub> = V <sub>SIM</sub>
Logic HIGH	2DAT = DAT, 2RST = RST, 2CLK = CLK, 2V <sub>SIM</sub> = V <sub>SIM</sub>

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	+5.5	V
$V_{CNTRL}$	DC Input Voltage (Sel) <sup>(1)</sup>	-0.5	$V_{CC}$	V
$V_{SW}$	DC Switch I/O Voltage <sup>(1)</sup>	-0.5	$V_{CC} + 0.3$	V
$I_{IK}$	DC Input Diode Current	-50		mA
$I_{SIM}$	DC Output Current - $V_{SIM}$		350	mA
$I_{OUT}$	DC Output Current – DAT, CLK, RST		35	mA
$T_{STG}$	Storage Temperature	-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	3	kV
		I/O to GND	12	
	Charged Device Model, JEDEC: JESD22-C101		2	

### Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	1.65	4.30	V
$V_{CNTRL}$	Control Input Voltage (Sel) <sup>(2)</sup>	0	$V_{CC}$	V
$V_{SW}$	Switch I/O Voltage	-0.5	$V_{CC}$	V
$I_{SIM}$	DC Output Current - $V_{SIM}$		150	mA
$I_{OUT}$	DC Output Current – DAT, CLK, RST		25	mA
$T_A$	Operating Temperature	-40	+85	°C

### Note:

- The control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

All typical values are at 25°C, 3.3 V  $V_{CC}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN} = -18 \text{ mA}$	2.7			-1.2	V
$V_{IH}$	Input Voltage High		1.65 to 2.3	1.1			V
			2.7 to 3.6	1.3			
			4.3	1.7			
$V_{IL}$	Input Voltage Low		1.65 to 2.3			0.4	V
			2.7 to 3.6			0.5	
			4.3			0.7	
$I_{IN}$	Control Input Leakage	$V_{SW} = 0 \text{ to } V_{CC}$	4.3	-1		1	$\mu\text{A}$
$I_{nc(off)}, I_{no(off)}$	Off State Leakage	$nRST, nDAT, nCLK, nV_{SIM} = 0.3 \text{ V}$ or 3.6 V Figure 10	4.3	-60		60	nA
$R_{OND}$	Data Path Switch On Resistance <sup>(3)</sup>	$V_{SW} = 0, 1.8 \text{ V}, I_{ON} = -20 \text{ mA}$ Figure 9	1.8		7.0	12.0	$\Omega$
		$V_{SW} = 0, 2.3 \text{ V}, I_{ON} = -20 \text{ mA}$ Figure 9	2.7		6.0	10.0	
$R_{ONV}$	$V_{SIM}$ Switch On Resistance <sup>(3)</sup>	$V_{SW} = 0, 1.8 \text{ V}, I_{ON} = -100 \text{ mA}$ Figure 9	1.8		0.5	0.7	$\Omega$
		$V_{SW} = 0, 2.3 \text{ V}, I_{ON} = -100 \text{ mA}$ Figure 9	2.7		0.4	0.6	
$\Delta R_{OND}$	Data Path Delta On Resistance <sup>(4)</sup>	$V_{SW} = 0 \text{ V}, I_{ON} = -20 \text{ mA}$	2.7		0.2		$\Omega$
$I_{CC}$	Quiescent Supply Current	$V_{CNTRL} = 0 \text{ or } V_{CC}, I_{OUT} = 0$	4.3			1.0	$\mu\text{A}$
$I_{CCT}$	Increase in $I_{CC}$ Current Per Control Voltage and $V_{CC}$	$V_{CNTRL} = 2.6 \text{ V}, V_{CC} = 4.3 \text{ V}$	4.3		5.0	10.0	$\mu\text{A}$
		$V_{CNTRL} = 1.8 \text{ V}, V_{CC} = 4.3 \text{ V}$	4.3		7.0	15.0	$\mu\text{A}$

**Notes:**

3. Measured by the voltage drop between nDAT, nRST, nCLK and relative common port pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the relative ports.
4. Guaranteed by characterization.

## AC Electrical Characteristics

All typical value are for  $V_{CC}=3.3V$  at  $25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Units
				Min.	Typ.	Max.	
$t_{OND}$	Turn-On Time Sel to Output (DAT,CLK,RST)	$R_L = 50 \Omega, C_L = 35 \text{ pF}$ $V_{SW} = 1.5 \text{ V}$ Figure 11, Figure 12	$1.8^{(5)}$		65	95	ns
			2.7 to 3.6		42	60	ns
$t_{OFFD}$	Turn-Off Time Sel to Output (DAT,CLK,RST)	$R_L = 50 \Omega, C_L = 35 \text{ pF}$ $V_{SW} = 1.5 \text{ V}$ Figure 11, Figure 12	$1.8^{(5)}$		30	50	ns
			2.7 to 3.6		20	40	ns
$t_{ONV}$	Turn-On Time Sel to Output ( $V_{SIM}$ )	$R_L = 50 \Omega, C_L = 35 \text{ pF}$ $V_{SW} = 1.5 \text{ V}$ Figure 11, Figure 12	$1.8^{(5)}$		55	80	ns
			2.7 to 3.6		35	55	ns
$t_{OFFV}$	Turn-Off Time Sel to Output ( $V_{SIM}$ )	$R_L = 50 \Omega, C_L = 35 \text{ pF}$ $V_{SW} = 1.5 \text{ V}$ Figure 11, Figure 12	$1.8^{(5)}$		35	50	
			2.7 to 3.6		22	40	ns
$t_{PD}$	Propagation Delay <sup>(5)</sup> (DAT,CLK,RST)	$C_L = 35 \text{ pF}, R_L = 50 \Omega$ Figure 11, Figure 13	3.3		0.25		ns
$t_{BBMD}$	Break-Before-Make <sup>(5)</sup> (DAT,CLK,RST)	$R_L = 50 \Omega, C_L = 35 \text{ pF}$ $V_{SW1} = V_{SW2} = 1.5 \text{ V}$ Figure 15	2.7 to 3.6	3	18		ns
$t_{BBMV}$	Break-Before-Make <sup>(5)</sup> ( $V_{SIM}$ )	$R_L = 50 \Omega, C_L = 35 \text{ pF}$ $V_{SW1} = V_{SW2} = 1.5 \text{ V}$ Figure 15	2.7 to 3.6	3	12		ns
Q	Charge Injection (DAT,CLK,RST)	$C_L = 50 \text{ pF}, R_{GEN} = 0 \Omega,$ $V_{GEN} = 0 \text{ V}$	2.7 to 3.6		10		pC
$O_{IRR}$	Off Isolation (DAT,CLK,RST)	$R_L = 50 \Omega, f = 10 \text{ MHz}$ Figure 17	2.7 to 3.6		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk (DAT,CLK,RST)	$R_L = 50 \Omega, f = 10 \text{ MHz}$ Figure 18	2.7 to 3.6		-60		dB
BW	-3 db Bandwidth (DAT,CLK,RST)	$R_L = 50 \Omega, C_L = 5 \text{ pF}$ Figure 16	2.7 to 3.6		475		MHz

**Note:**

- Guaranteed by characterization.

## Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> = -40°C to +85°C			Units
			Min.	Typ.	Max.	
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 0 V		1.5		pF
C <sub>OND</sub>	RST, CLK, DAT On Capacitance <sup>(6)</sup>	V <sub>CC</sub> = 3.3 V, f = 1 MHz Figure 20		10	12	
C <sub>ONV</sub>	V <sub>SIM</sub> On Capacitance <sup>(6)</sup>	V <sub>CC</sub> = 3.3 V, f = 1 MHz Figure 20		110	150	
C <sub>OFFD</sub>	RST, CLK, DAT Off Capacitance	V <sub>CC</sub> = 3.3 V, Figure 19		3		
C <sub>OFFV</sub>	V <sub>SIM</sub> Off Capacitance	V <sub>CC</sub> = 3.3 V, Figure 19		40		

**Note:**

6. Guaranteed by characterization.

Typical Performance Characteristics

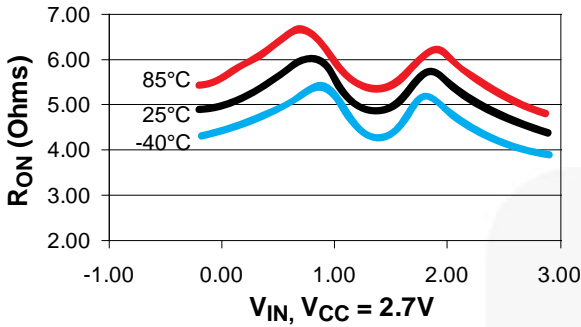


Figure 4.  $R_{ON}$  Data Path

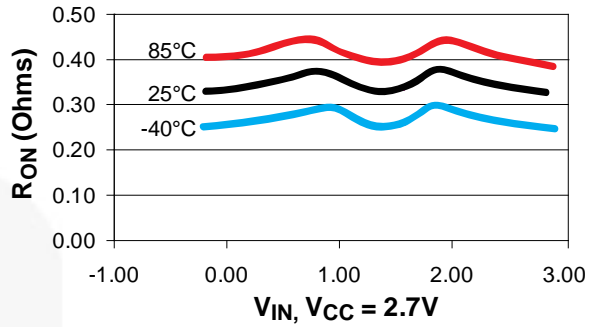


Figure 5.  $R_{ON}$   $V_{SIM}$

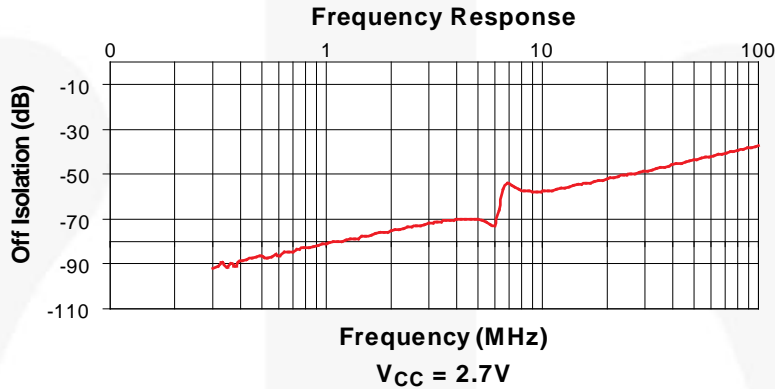


Figure 6. Off Isolation

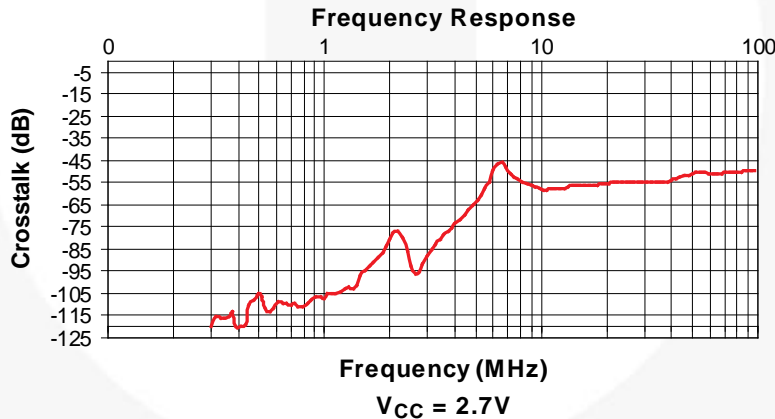


Figure 7. Crosstalk

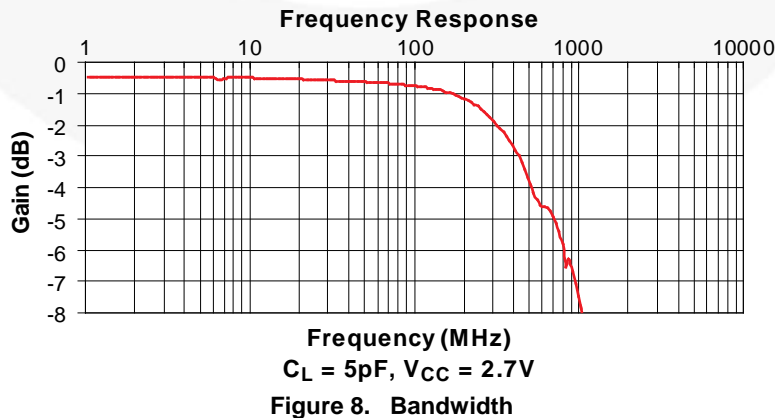
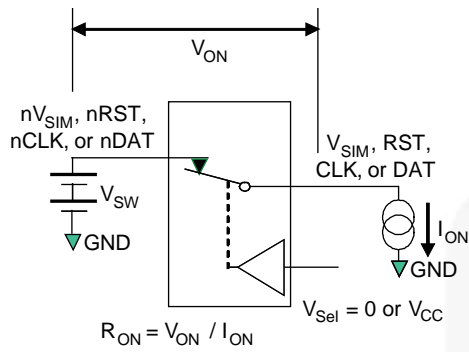
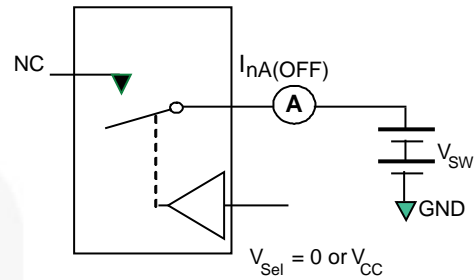


Figure 8. Bandwidth

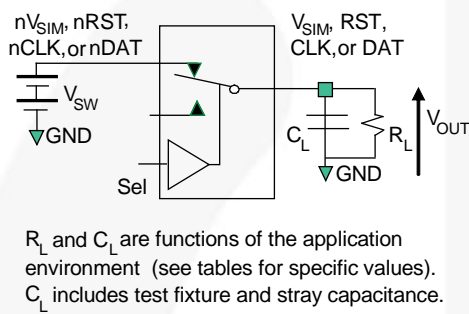
## Test Diagrams



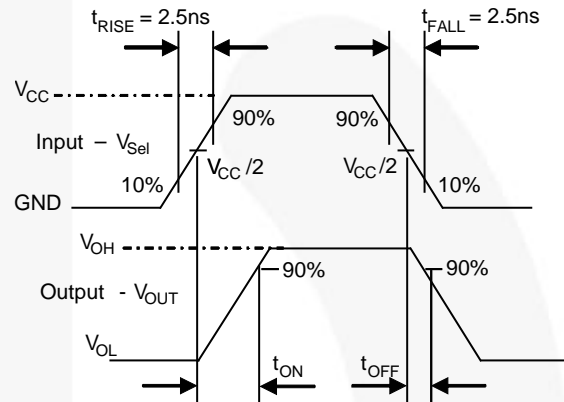
**Figure 9. On Resistance**



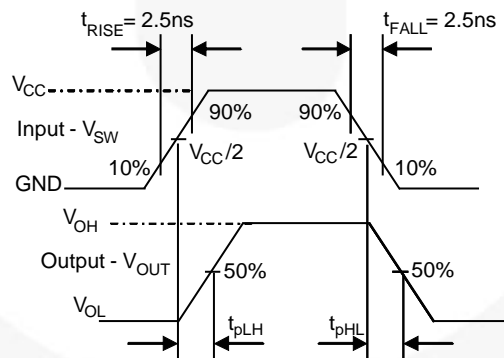
**Figure 10. Off Leakage**



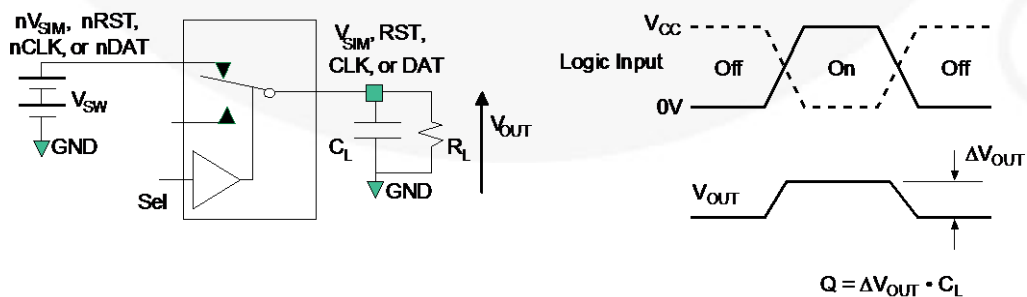
**Figure 11. AC Test Circuit Load**



**Figure 12. Turn-On / Turn-Off Waveforms**



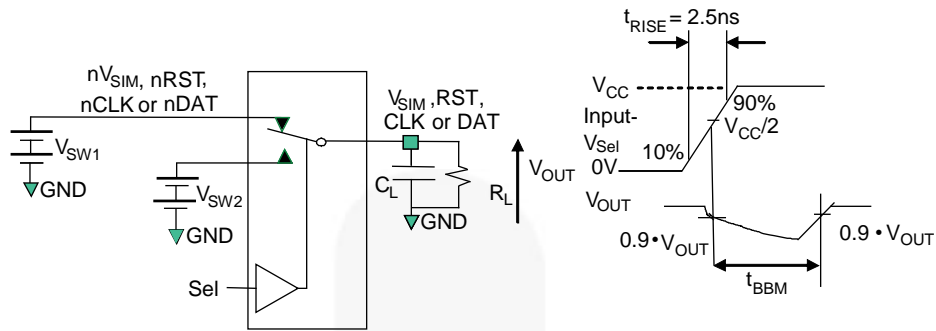
**Figure 13. Propagation Delay**



**Figure 14. Charge Injection**

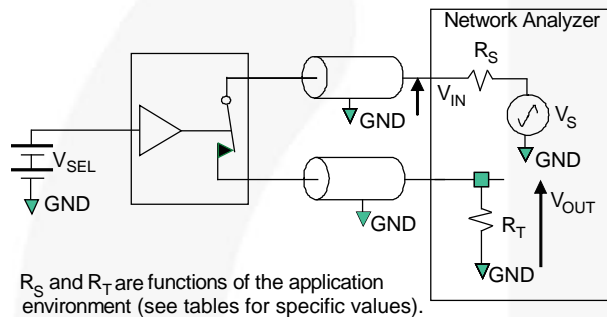


**Test Diagrams (Continued)**



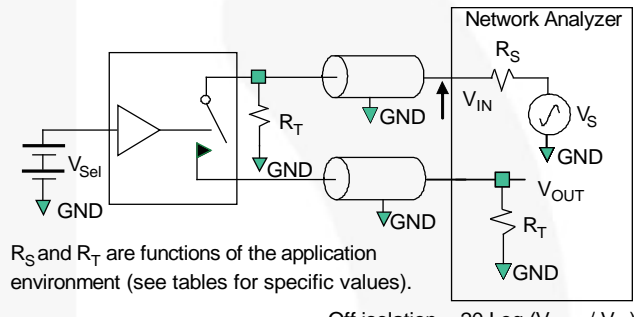
$R_L$  and  $C_L$  are functions of the application environment (see tables for specific values).  $C_L$  includes test fixture and stray capacitance.

**Figure 15. Break-Before-Make Interval Timing**



$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

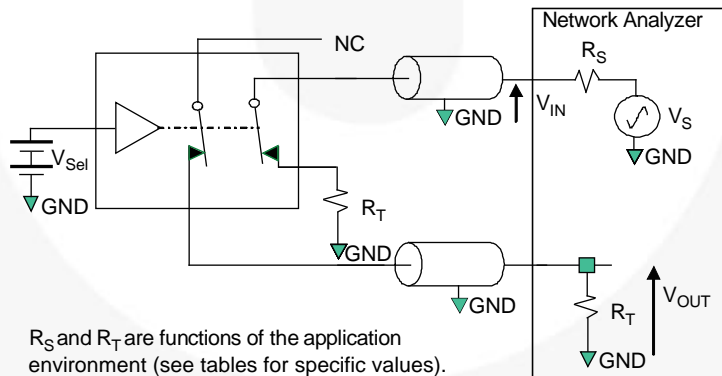
**Figure 16. Bandwidth**



$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

Off isolation =  $20 \text{ Log } (V_{OUT} / V_{IN})$

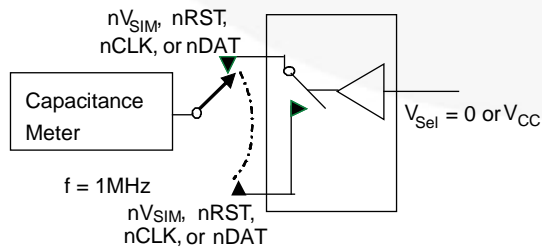
**Figure 17. Channel Off Isolation**



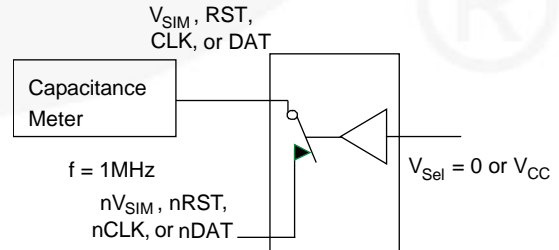
$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

Crosstalk =  $20 \text{ Log } (V_{OUT} / V_{IN})$

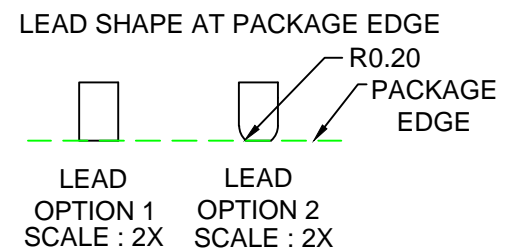
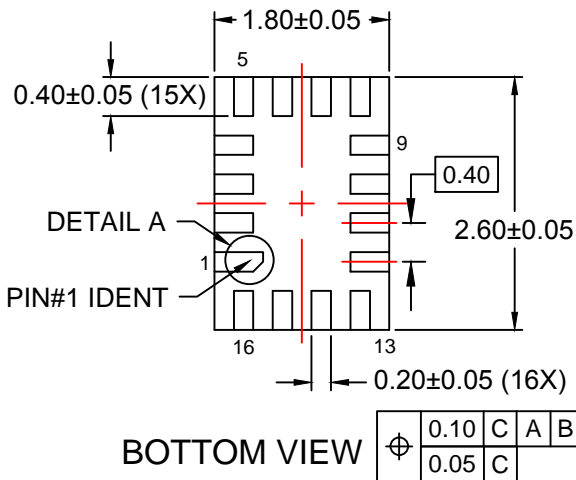
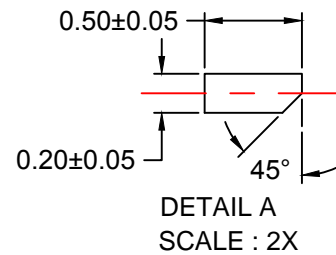
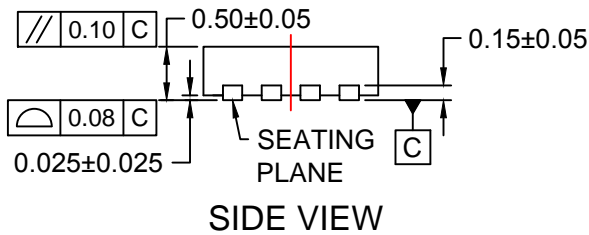
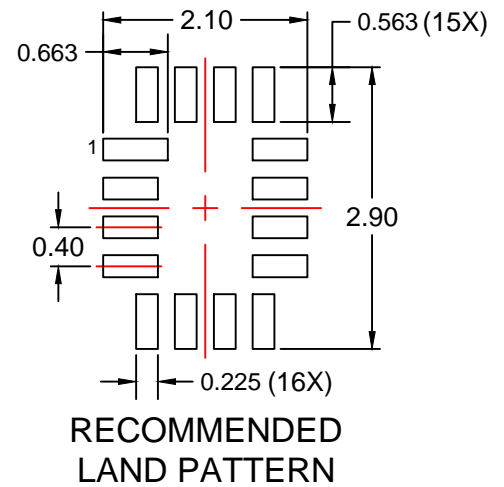
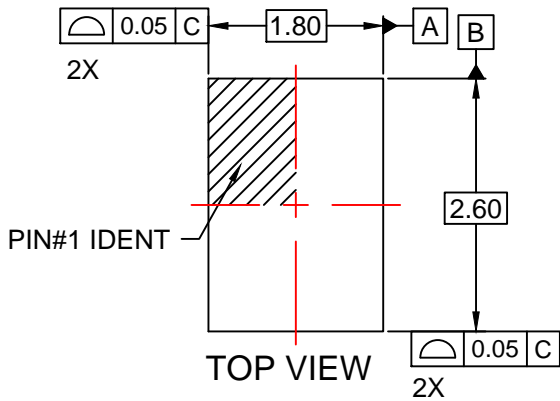
**Figure 18. Non-Adjacent Channel-to-Channel Crosstalk**



**Figure 19. Channel Off Capacitance**



**Figure 20. Channel On Capacitance**



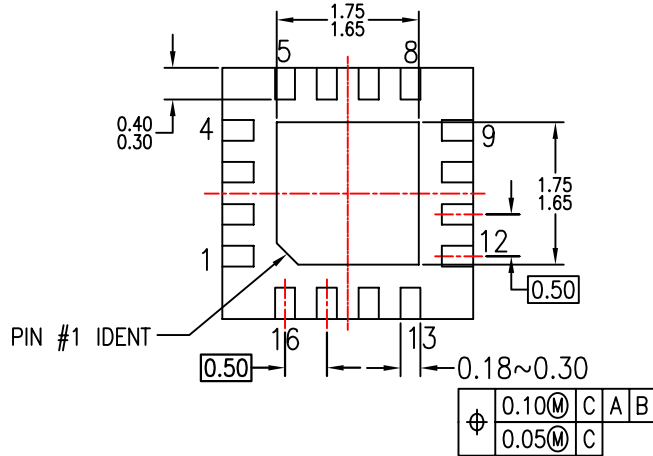
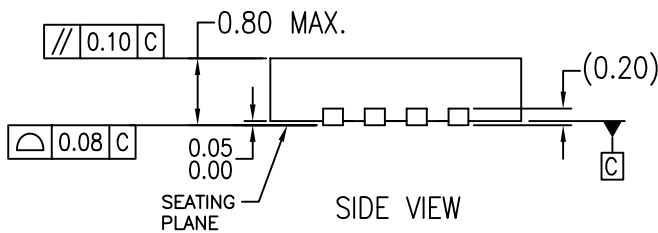
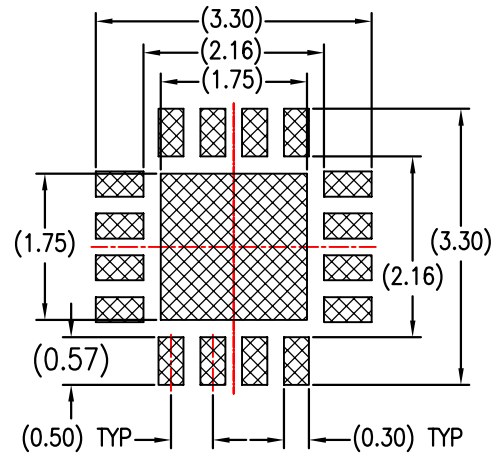
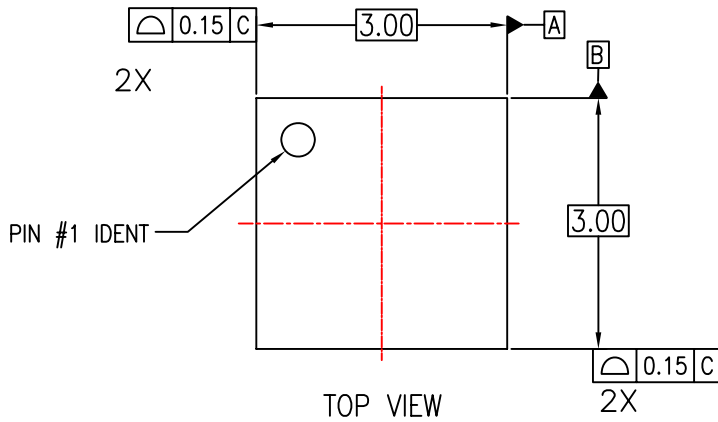
**NOTES:**

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-UMLP16Arev5.
- F. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.



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REVISIONS				
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	ECN-MKT-MLP16B	21-2-05	FEITAN
B	Lead length Changed from 0.35-0.45 to 0.30-0.40	ECN-MKT-MLP16B revB	10-6-05	Jkingsbury



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WEED-Pending, DATED pending
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MLP16BrevB

APPROVALS	DATE		Bayan Lepas, FIZ, 11900, Penang, Malaysia.		
DRAWN FEITAN	18-2-2005			16LD, MLP, QUAD, JEDEC MO-220, 3MM SQUARE	
DFTG. CHK. J. KINGSBURY	6-6-2005				
ENGR. CHK. D. CHONG	6-6-2005				
		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	N/A	MKT-MLP16B	B
DO NOT SCALE DRAWING				SHEET 1 of 1	



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EcoSPARK®	MicroFET™	Solutions for Your Success™	
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ESBC™	MicroPak2™	STEALTH™	Ultra FRFET™
	MillerDrive™	SuperFET®	UniFET™
Fairchild®	MotionMax™	SuperSOT™-3	VCX™
Fairchild Semiconductor®	MotionGrid®	SuperSOT™-6	VisualMax™
FACT Quiet Series™	MTI®	SuperSOT™-8	VoltagePlus™
FACT®	MTX®	SupreMOS®	XS™
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### ANTI-COUNTERFEITING POLICY

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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