INA21x-Q1 Automotive-Grade Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors

1 Features

- Qualified for Automotive Applications
- Wide Common-Mode Range: –0.3 V to 26 V
- Offset Voltage: ±100 µV (Maximum)
  (Enables Shunt Drops of 10-mV Full-Scale)
- Accuracy:
  - ±1% Gain Error (Maximum over Temperature)
  - 0.5-µV/°C Offset Drift (Maximum)
  - 10-ppm/°C Gain Drift (Maximum)
- Choice of Gain
  - INA212-Q1: 1000 V/V
  - INA213A-Q1: 50 V/V
  - INA214-Q1: 100 V/V
- Quiescent Current: 100 µA (Maximum)
- SC70 Package

2 Applications

- Body Control Module
- Valve Control
- Motor Control
- Electronic Stability Control
- Wireless Charging Transmitters

3 Description

The INA21x-Q1 devices are voltage-output, current-shunt monitors (also called current-sense amplifiers) that can sense drops across shunts at common-mode voltages from –0.3 V to 26 V, independent of the supply voltage. The INA212-Q1 offers a fixed gain of 1000 V/V, INA213A-Q1 offers a fixed gain of 50 V/V, and the INA214-Q1 offers a fixed gain of 100 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

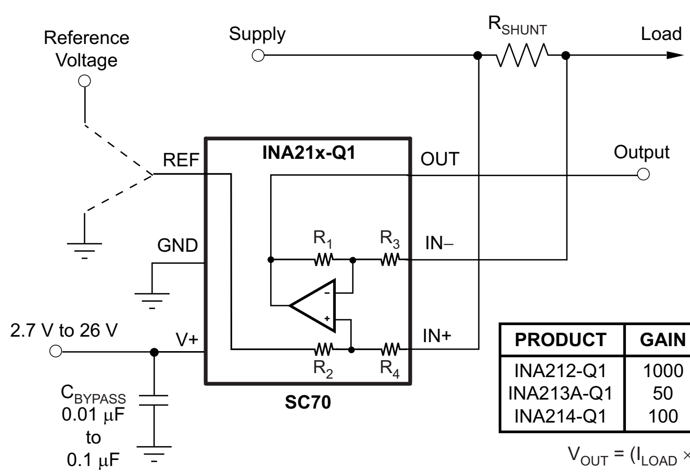
The devices operate from a single 2.7-V to 26-V power supply, drawing a maximum of 100 µA of supply current. They are specified over the operating temperature range of –40°C to 125°C and are offered in an SC70 package.

Device Information(1)

PART NUMBER	PACKAGE	GAIN (V/V)
INA212-Q1	SOT (6)	1000
INA213A-Q1		50
INA214-Q1		100

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



PRODUCT	GAIN	R_3 and R_4	R_1 and R_2
INA212-Q1	1000	1 kΩ	1 MΩ
INA213A-Q1	50	20 kΩ	1 MΩ
INA214-Q1	100	10 kΩ	1 MΩ

$V_{OUT} = (I_{LOAD} \times R_{SHUNT})\ \text{Gain} + V_{REF}$

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2013) to Revision E — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4
- Deleted θ_{JA} Thermal Resistance parameter from *Electrical Characteristics* 5

Changes from Revision C (August 2013) to Revision D — **Page**

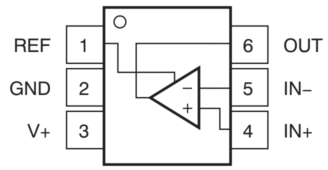
- Changed INA213-Q1 device to INA213A-Q1 device throughout document. 1
- Deleted T_A, Operating Temperature from *ABSOLUTE MAXIMUM RATINGS* table. 4

Changes from Revision B (June 2010) to Revision C — **Page**

- Changed device names to -Q1 throughout. 1
- Added INA212-Q1: 1000 V/V to Features. 1
- Changed this list to be all automotive specific 1
- Added INA212-Q1 offers a fixed gain of 1000 V/V to Description. 1
- Added INA212-Q1 to image. 1
- Removed Ordering Information table. 4
- Changed HBM to 2000 V, removed MM. 4
- Changed T_A to -40 to 125°C. 4
- Added INA212-Q1 values to CMRR V_{OS} and Gain in Electrical Characteristics table. 5
- Changed Bandwidth parameter in the *ELECTRICAL CHARACTERISTICS* to differentiate between devices 5
- Changed *GAIN vs FREQUENCY* graph to show difference between devices 6
- Added INA212-Q1 device name in App Information. 11
- Added INA212-Q1 to image. 13

5 Pin Configuration and Functions

DCK Package
SC70-6
(Top View)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
IN–	5	I	Connect to load side of shunt resistor.
IN+	4	I	Connect to supply side of shunt resistor
OUT	6	O	Output voltage
REF	1	I	Reference voltage, 0 V to V+
V+	3	—	Power supply, 2.7 V to 26 V

(1) Analog

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
Supply voltage, V_S			26	V
Analog inputs, V_{IN+} , $V_{IN–}$ (2)	Differential (V_{IN+})–($V_{IN–}$)	–26	26	V
	Common-Mode (3)	GND – 0.3	26	V
REF input		GND – 0.3	(V_S) + 0.3	V
Output (3)		GND – 0.3	(V_S) + 0.3	V
Input current into any terminal(3)			5	mA
Operating temperature		–55	150	°C
Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– terminals, respectively.
(3) Input voltage at any terminal may exceed the voltage shown if the current at that pin is limited to 5 mA.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (REF, GND, V+, and IN+)	–1000	1000	
			Other pins	–1000	1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Supply voltage	2.7		26	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA21x-Q1 DCK (SC70) 6 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	227.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	79.5	
$R_{θJB}$	Junction-to-board thermal resistance	72.1	
$ψ_{JT}$	Junction-to-top characterization parameter	3.6	
$ψ_{JB}$	Junction-to-board characterization parameter	70.4	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

$V_{SENSE} = V_{IN+} – V_{IN–}$, V_S = +5 V, V_{IN+} = 12 V, $V_{REF} = V_S/2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
INPUT								
V_{CM}	Common-mode input range			Full range	–0.3		26	V
CMRR	Common-mode rejection ratio	V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV	INA212-Q1	Full range	100	140		dB
			INA213A-Q1		100	120		
			INA214-Q1		100	140		
V_{OS}	Offset voltage	RTI (2), V_{SENSE} = 0 mV	INA212-Q1	25°C		±0.55	±35	µV
			INA213A-Q1			±5	±100	
			INA214-Q1			±1	±60	
dV_{OS}/dT	Offset voltage vs temperature (3)			Full range		0.1	0.5	µV/°C
PSR	Offset voltage vs power supply	V_S = 2.7 V to 18 V, V_{IN+} = 18 V, V_{SENSE} = 0 mV		25°C		±0.1	±10	µV/V
I_B	Input bias current	V_{SENSE} = 0 mV		25°C	15	28	35	µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		25°C		±0.02		µA
OUTPUT								
	Gain	INA212-Q1				1000		V/V
		INA213A-Q1				50		
		INA214-Q1				100		
	Gain error	V_{SENSE} = –5 mV to 5 mV		Full range		±0.02%	±1%	
	Gain error vs temperature (3)			Full range		3	10	ppm/°C
	Nonlinearity error	V_{SENSE} = –5 mV to 5 mV		25°C		±0.01%		
	Maximum capacitive load	No sustained oscillation		25°C		1		nF
VOLTAGE OUTPUT								
	Output voltage swing to V+ power-supply rail (4)	R_L = 10 kΩ to GND		Full range		(V+) – 0.05	(V+) – 0.2	V
	Output voltage swing to GND			Full range		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE								
BW	Bandwidth	C_{LOAD} = 10 pF, INA212		25°C		4		kHz
		C_{LOAD} = 10 pF, INA213A				80		
		C_{LOAD} = 10 pF, INA214				30		
SR	Slew rate			25°C		0.4		V/µs
NOISE, RTI								
	Voltage noise density	RTI (2)		25°C		25		nV/√Hz
POWER SUPPLY								
I_Q	Quiescent current	V_{SENSE} = 0 mV		25°C		65	100	µA
				Full range			115	

(1) Full range T_A = –40°C to 125°C
(2) RTI = referred to input
(3) Not production tested
(4) See Typical Characteristic, *Output Voltage Swing vs Output Current* (Figure 10).

6.6 Typical Characteristics

T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S/2 (unless otherwise noted)

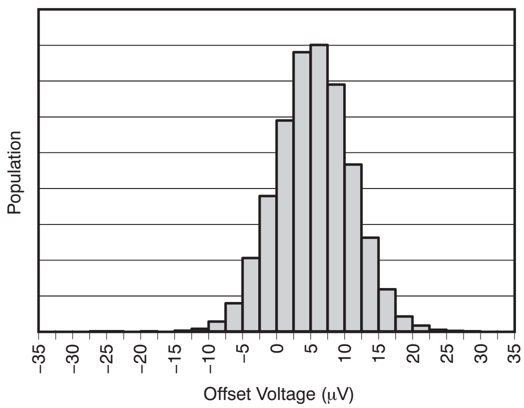


Figure 1. Input Offset Voltage Production Distribution

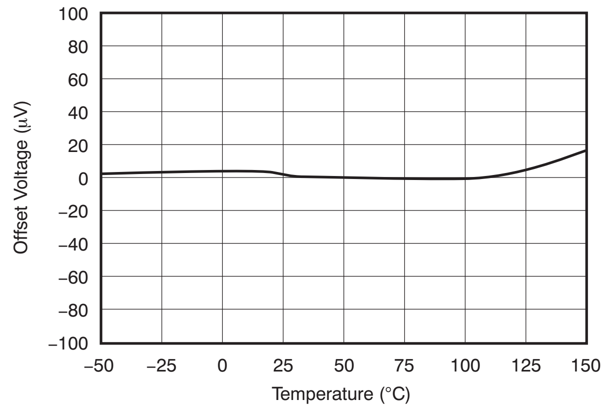


Figure 2. Offset Voltage vs Temperature

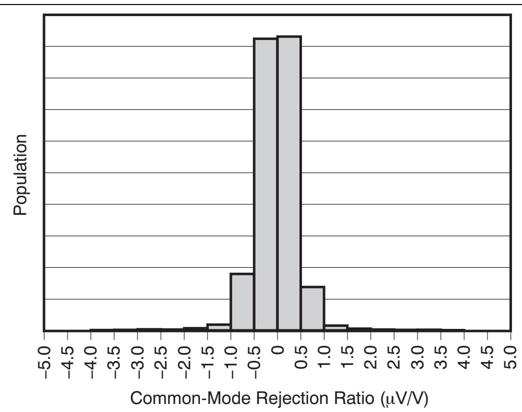


Figure 3. Common-Mode Rejection Production Distribution

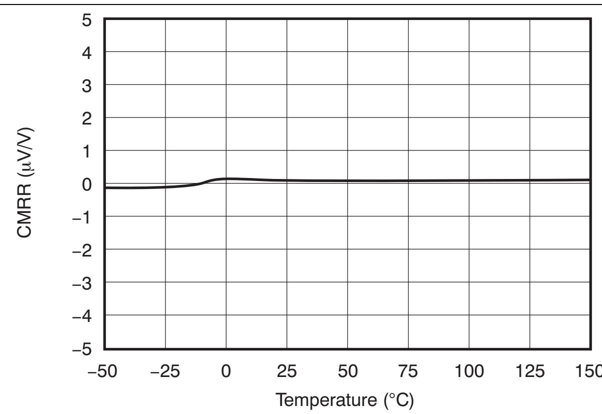


Figure 4. Common-Mode Rejection Ratio vs Temperature

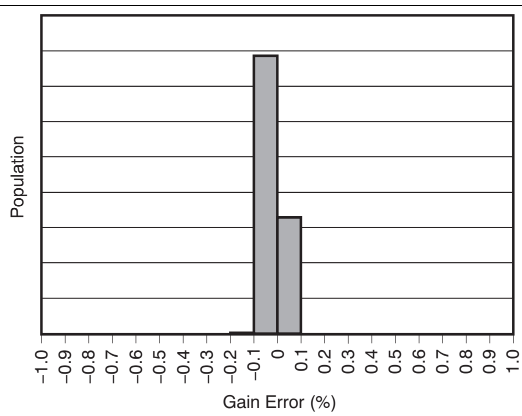


Figure 5. Gain Error Production Distribution

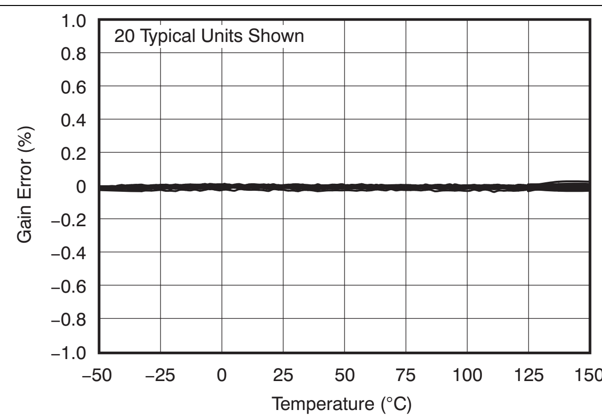


Figure 6. Gain Error vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S/2 (unless otherwise noted)

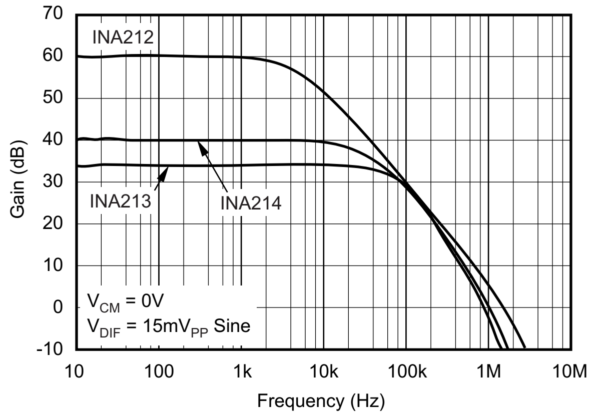


Figure 7. Gain vs Frequency

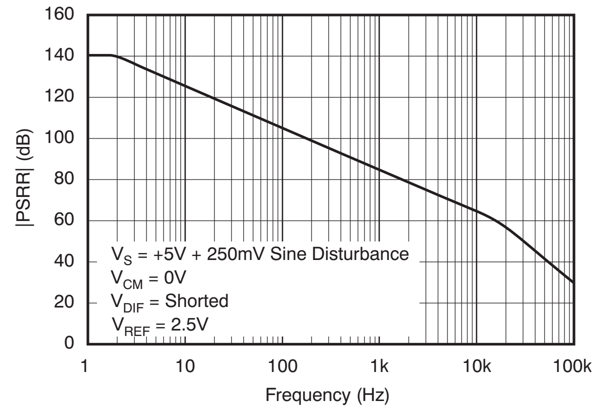


Figure 8. Power-Supply Rejection Ratio vs Frequency

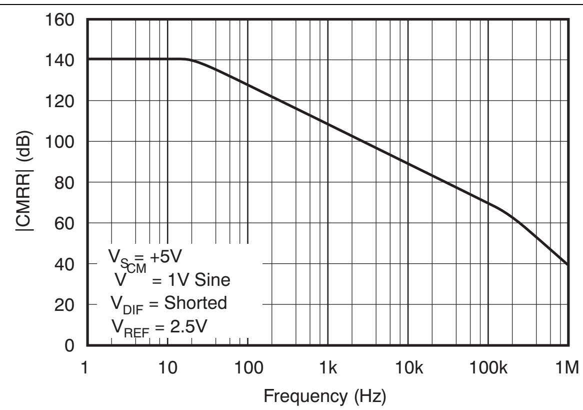


Figure 9. Common-Mode Rejection Ratio vs Frequency

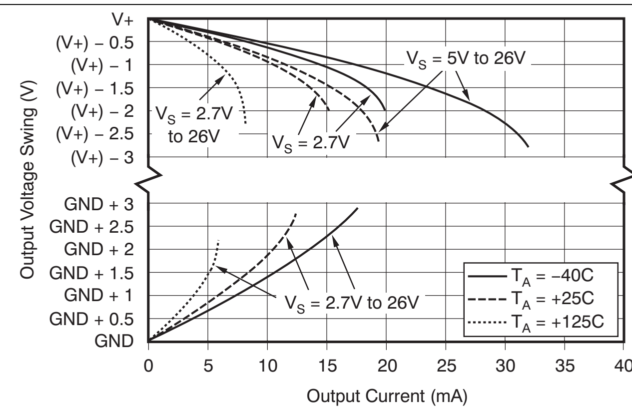


Figure 10. Output Voltage Swing vs Output Current

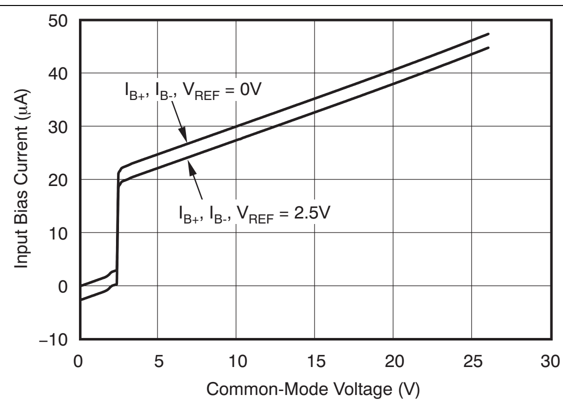


Figure 11. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 5 V

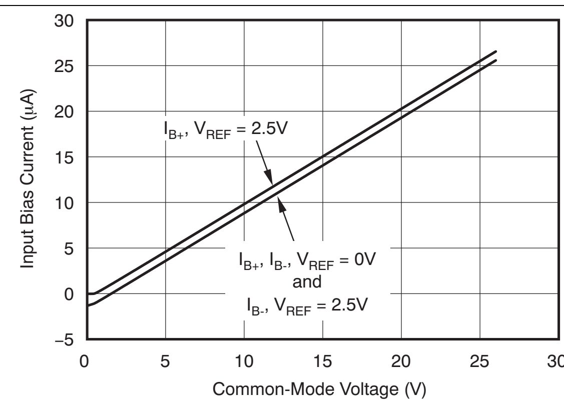


Figure 12. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 0 V (Shutdown)

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S/2 (unless otherwise noted)

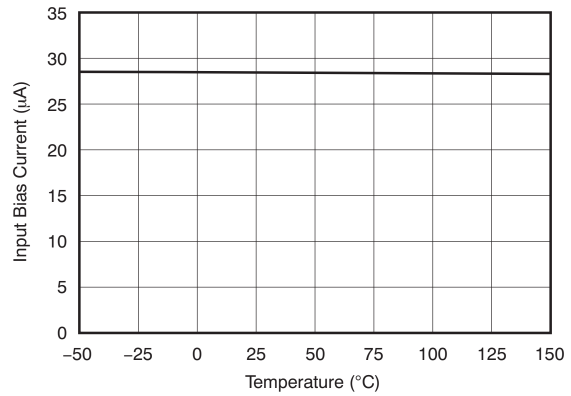


Figure 13. Input Bias Current vs Temperature

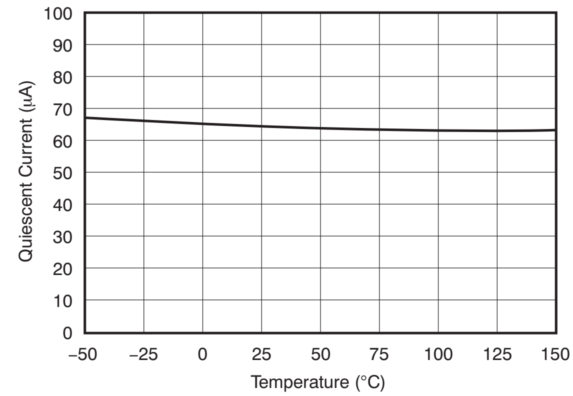


Figure 14. Quiescent Current vs Temperature

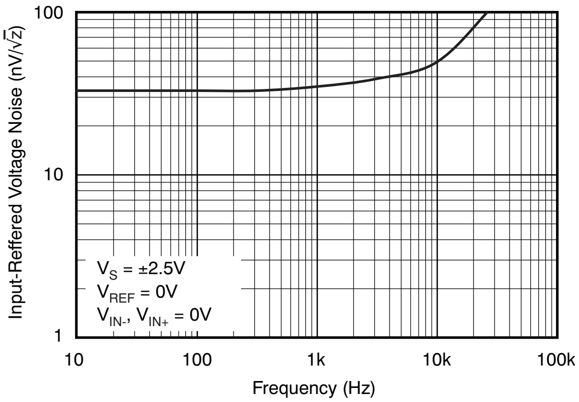


Figure 15. Input-Referred Voltage Noise vs Frequency

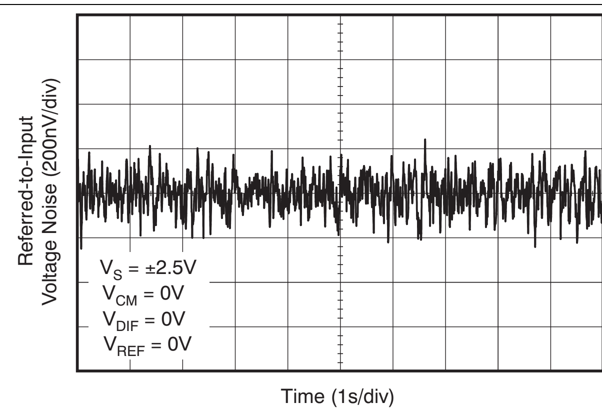


Figure 16. 0.1-Hz To 10-Hz Voltage Noise (Referred-To-Input)

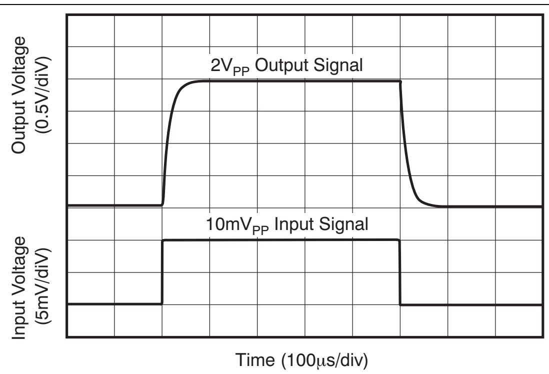


Figure 17. Step Response (10-mV$_{PP}$ Input Step)

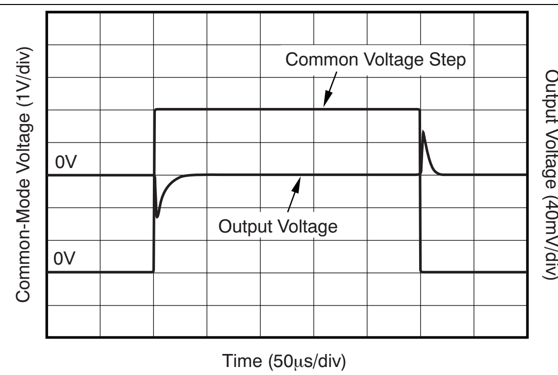


Figure 18. Common-Mode Voltage Transient Response

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S/2 (unless otherwise noted)

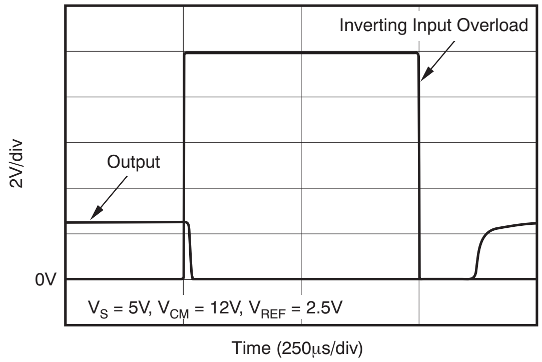


Figure 19. Inverting Differential Input Overload

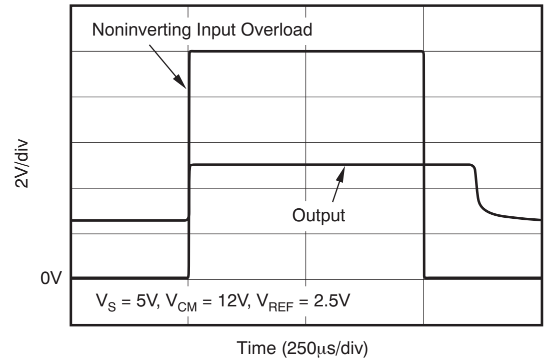


Figure 20. Noninverting Differential Input Overload

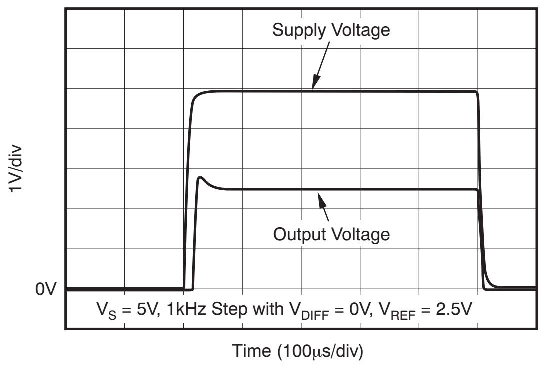


Figure 21. Start-Up Response

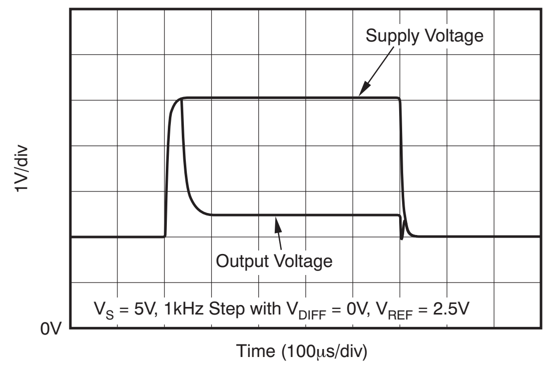


Figure 22. Brownout Recovery

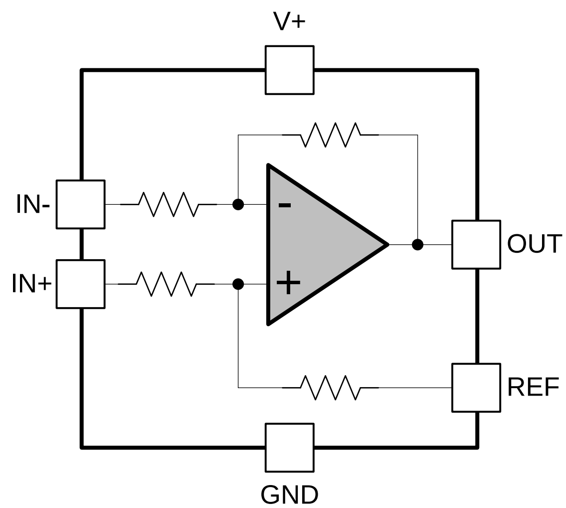
7 Detailed Description

7.1 Overview

The INA212-Q1, INA213A-Q1, and INA214-Q1 are 26-V, common-mode, zero-drift topology, current-sensing amplifiers that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V while the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 35 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Connections

Figure 23 shows the basic connections of the INA212-Q1, INA213A-Q1, or INA214-Q1. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

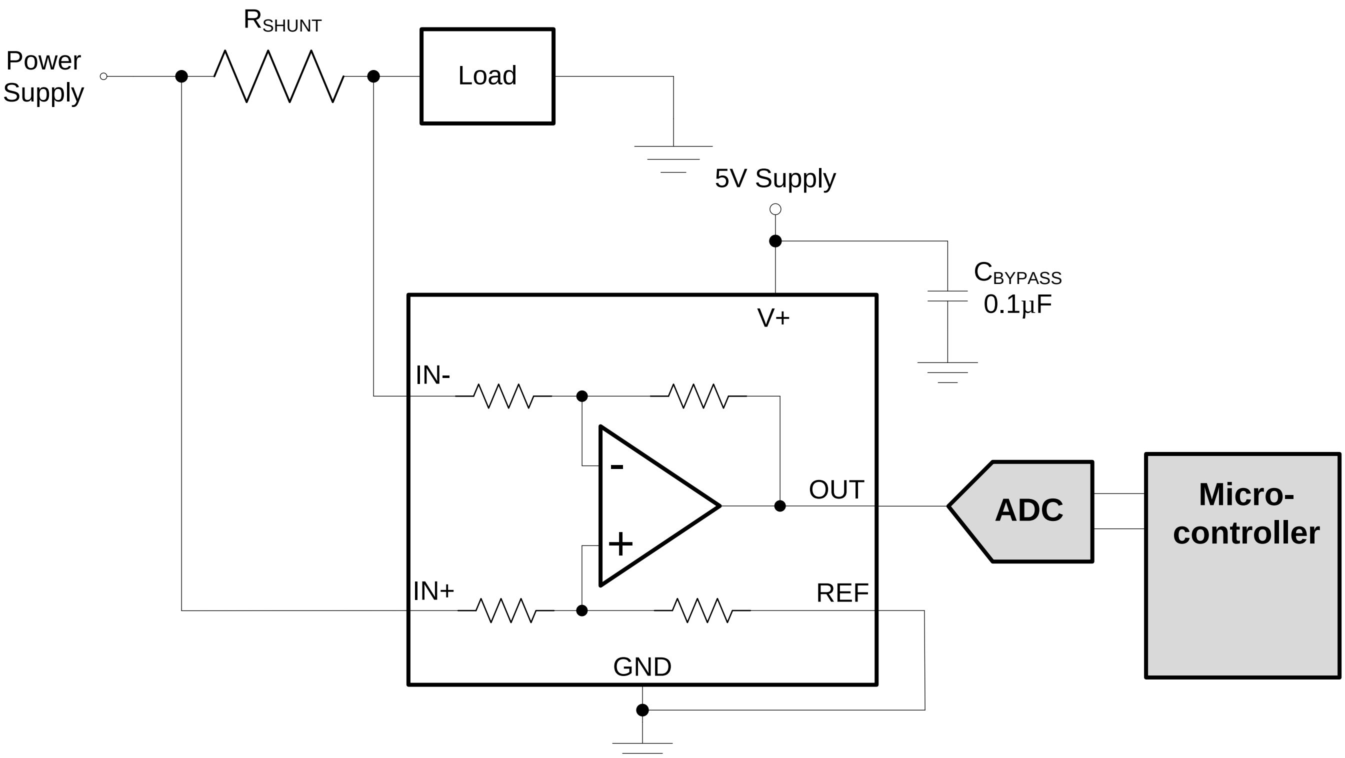


Figure 23. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

7.3.2 Selecting R_S

The zero-drift offset performance of the INA21x-Q1 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100 mV.

The INA21x-Q1 gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gain INA212-Q1, INA213A-Q1 or INA214-Q1 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA213A-Q1 operating on a 3.3-V supply could easily handle a full-scale shunt drop of 60 mV, with only 100 µV of offset.

7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA21x-Q1. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the input pins of the INA21x-Q1. This location, though, requires consideration of the ±30% tolerance of the internal resistances. Figure 24 shows a filter placed at the input pins.

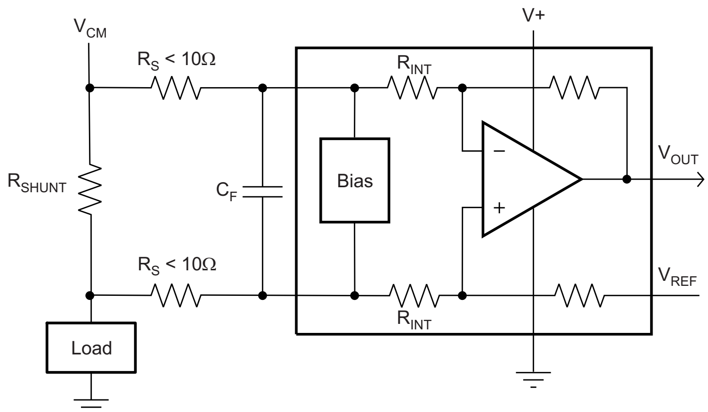


Figure 24. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in Figure 24 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 24). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})}$$

where:

- R_{INT} is the internal input resistor (R3 and R4), and
- R_S is the external series resistance. (1)

Device Functional Modes (continued)

With the adjustment factor from Equation 1 including the device internal input resistance, this factor varies with each gain version, as shown in Table 1. Each individual device gain error factor is shown in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN (V/V)	R_3 AND R_4 (kΩ)
INA212-Q1	1000	1
INA213A-Q1	50	20
INA214-Q1	100	10

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA212-Q1	$\frac{5000}{(9 \times R_S) + 5000}$
INA213A-Q1	$\frac{20,000}{(17 \times R_S) + 20,000}$
INA214-Q1	$\frac{10,000}{(9 \times R_S) + 10,000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

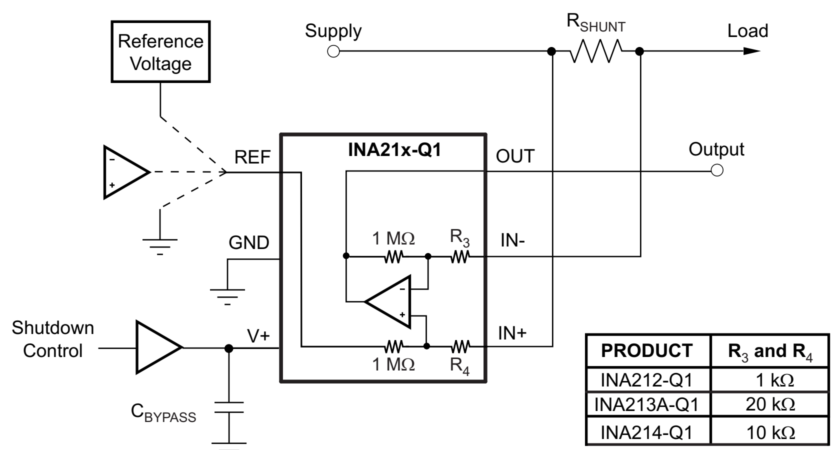
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA212-Q1 and the corresponding gain error equation from Table 2, a series resistance of 10 Ω results in a gain error factor of 0.982. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 1.77% solely because of the external 10-Ω series resistors. Using an INA213A-Q1 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

7.4.2 Shutting Down the INA21x-Q1 Series

While the INA21x-Q1 series does not have a shutdown pin, its low power consumption allows the output of a logic gate or transistor switch to power the INA21x-Q1. This gate or switch turns on and turns off the INA21x-Q1 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA21x-Q1 in shutdown mode shown in Figure 25.



NOTE: 1-MΩ paths from shunt inputs to reference and INA21x-Q1outputs.

Figure 25. Basic Circuit for Shutting Down INA21x-Q1 With a Grounded Reference

Note that there is typically slightly more than 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) from each input of the INA21x-Q1 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered while the INA21x-Q1 is shut down, the calculation is direct; instead of assuming 1 MΩ to ground, however, assume 1 MΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves as an open circuit when it is unpowered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA21x-Q1 does constitute a good path to ground; consequently, this current is directly proportional to a shunt common-mode voltage present across a 1-MΩ resistor.

As a final note, when the device is powered up, there is an additional, nearly constant and well-matched 25 µA that flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

7.4.3 REF Input Impedance Effects

As with any difference amplifier, the INA21x-Q1 common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin should be buffered by an op amp.

In systems where the INA21x-Q1 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 26 depicts a method of taking the output from the INA21x-Q1 by using the REF pin as a reference.

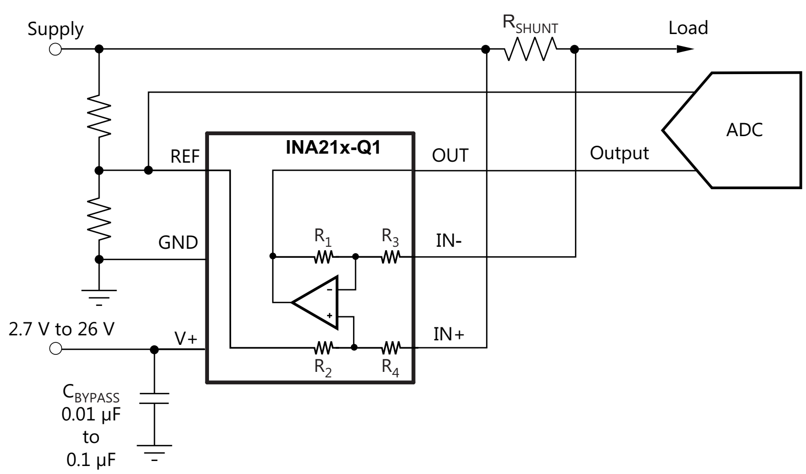


Figure 26. Sensing INA21x-Q1 to Cancel Effects of Impedance on the REF Input

7.4.4 Using the INA21x-Q1 with Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA21x-Q1 can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only zener diode or zener-type transient absorbers (sometimes referred to as *Transzorbs*) — any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the zener' see Figure 27. Keeping these resistors as small as possible is preferable, most often around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Input Filtering* section. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

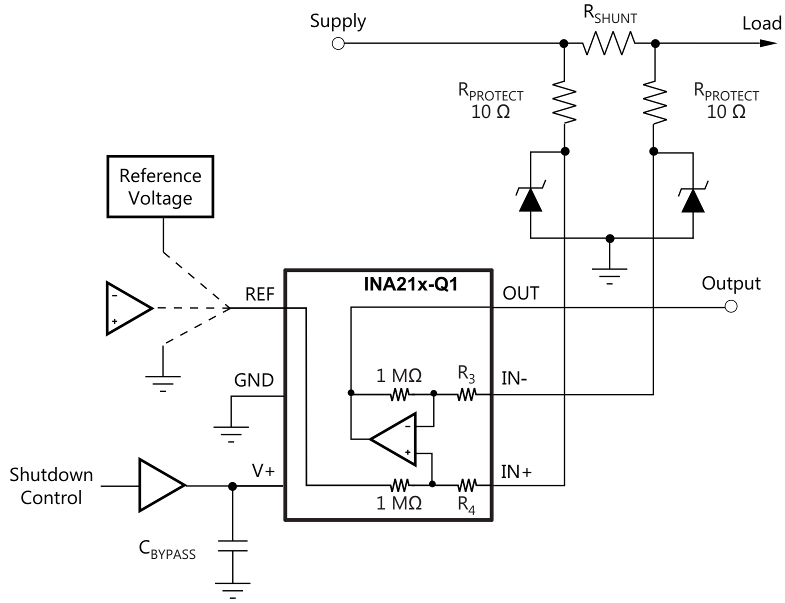


Figure 27. INA21x-Q1 Transient Protection Using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is shown in Figure 28. In either of these examples, the total board area required by the INA21x-Q1 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

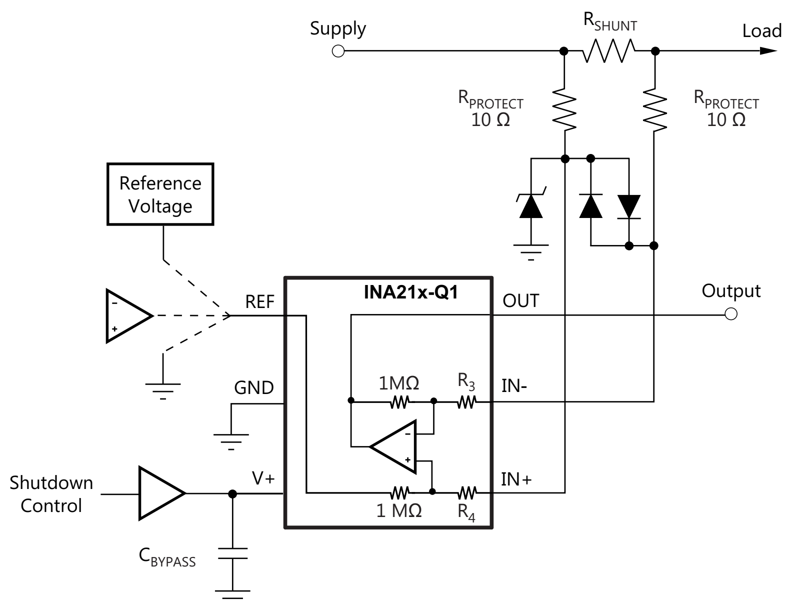


Figure 28. INA21x-Q1 Transient Protection Using a Single Transzorb and Input Clamps

7.4.5 Improving Transient Robustness

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins may cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Care must be taken to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, keep these resistances under 10 Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10 Ω of resistance at dc and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 µF and 0.1 µF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 29.

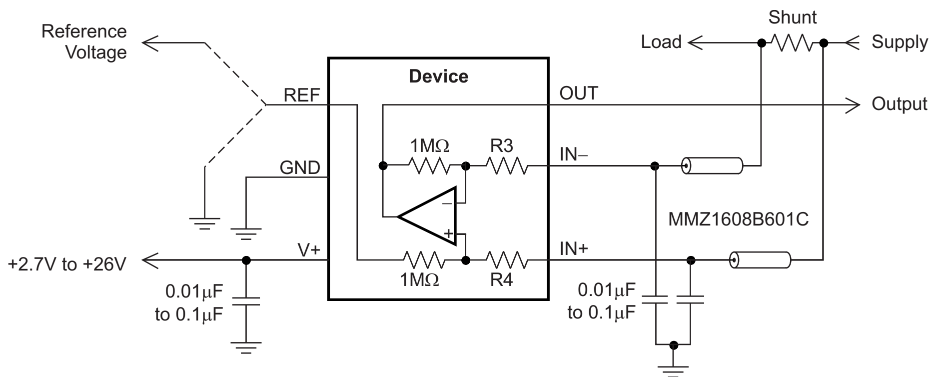


Figure 29. Transient Protection

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA21x-Q1 devices measure the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

8.2 Typical Applications

8.2.1 Unidirectional Operation

Unidirectional operation allows the INA21x-Q1 to measure currents through a resistive shunt in one direction. The most frequent case of unidirectional operation sets the output at ground by connecting the REF pin to ground. In unidirectional applications where the highest possible accuracy is desirable at very low inputs, bias the REF pin to a convenient value above 50 mV to get the device output swing into the linear range for zero inputs.

A less frequent case of unipolar output biasing is to bias the output by connecting the REF pin to the supply; in this case, the quiescent output for zero input is at quiescent supply. This configuration would only respond to negative currents (inverted voltage polarity at the device input).

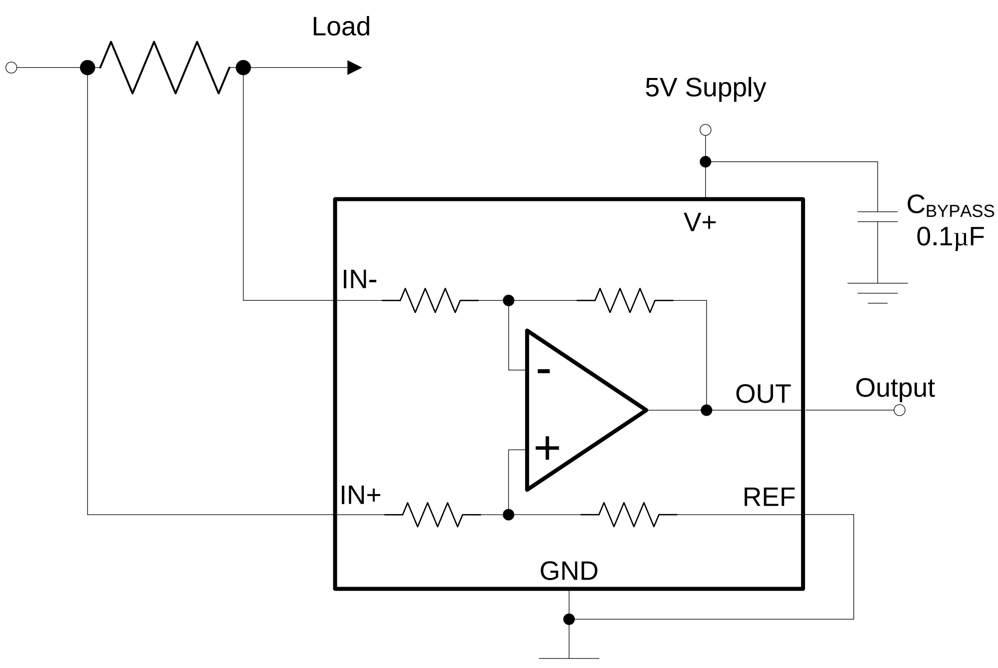


Figure 30. Unidirectional Application Schematic

8.2.1.1 Design Requirements

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 30. When the input signal increases, the output voltage at the OUT pin increases.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

8.2.1.3 Application Curve

An example output response of a unidirectional configuration is shown in Figure 31. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

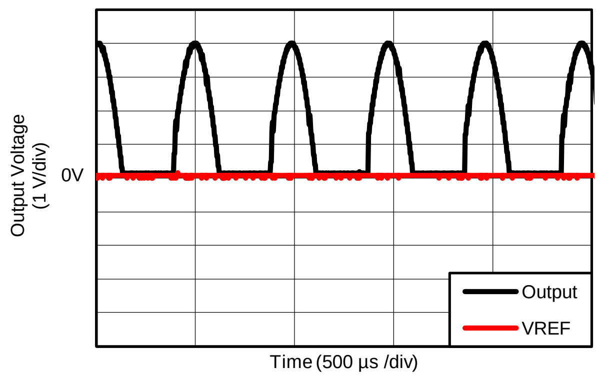


Figure 31. Unidirectional Application Output Response

Typical Applications (continued)

8.2.2 Bidirectional Operation

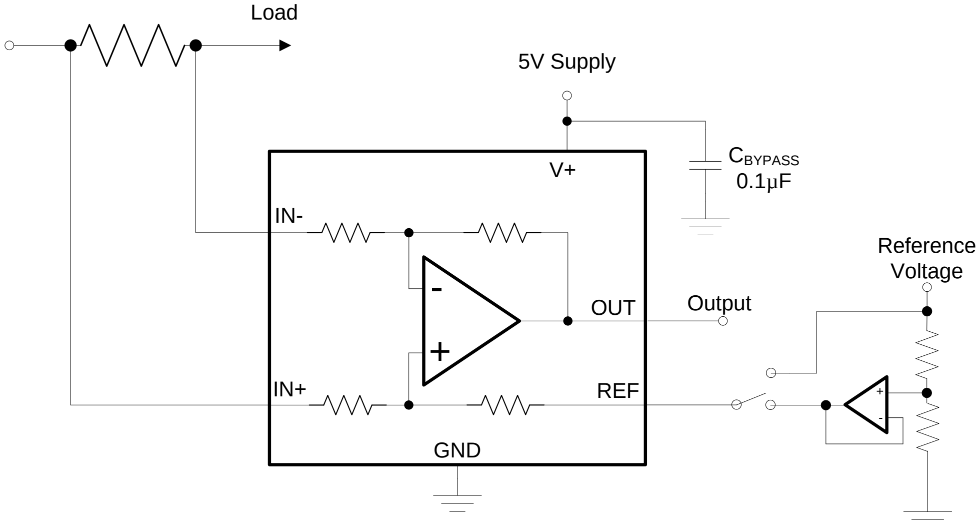


Figure 32. Bidirectional Application Schematic

8.2.2.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

8.2.2.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 32. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

8.2.2.3 Application Curve

An example output response of a bidirectional configuration is shown in Figure 33. With the REF pin connected to a reference voltage, 2.5 V in this case, the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals.

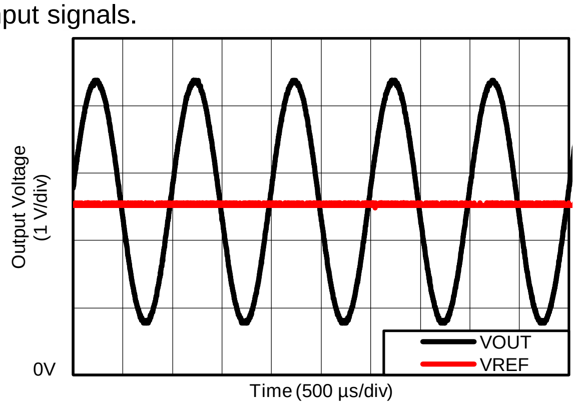


Figure 33. Bidirectional Application Output Response

9 Power Supply Recommendations

The input circuitry of the INA21x-Q1 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power supply voltage can be as high as 26 V. However, the output voltage range of the OUT terminal is limited by the voltages on the power-supply pin. Note also that the INA21x-Q1 can withstand the full input signal range up to 26 V at the input pins, regardless of whether the device has power applied or not.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

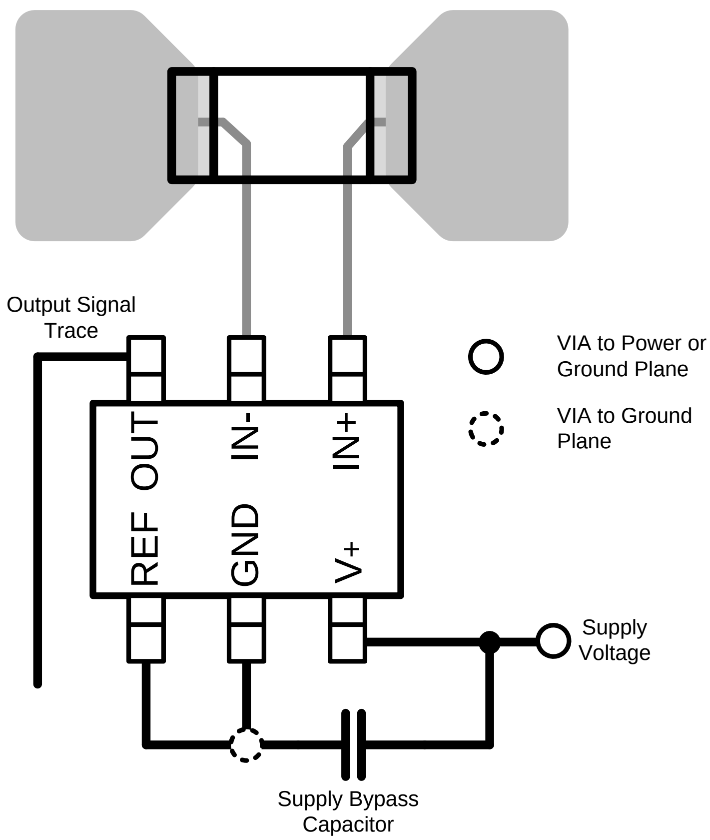


Figure 34. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- INA210-215EVM User's Guide, SBOU065

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA212-Q1	Click here	Click here	Click here	Click here	Click here
INA213A-Q1	Click here	Click here	Click here	Click here	Click here
INA214-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA212AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJW	Samples
INA213AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBX	Samples
INA214AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA212-Q1, INA214-Q1 :

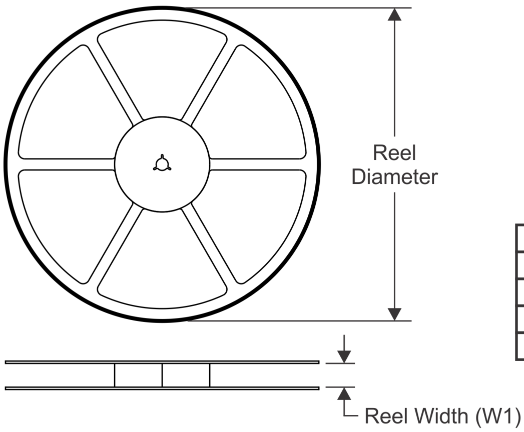
- Catalog: INA212, INA214

NOTE: Qualified Version Definitions:

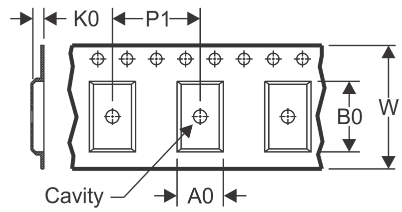
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

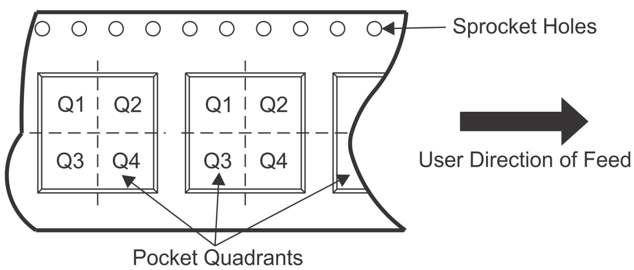


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

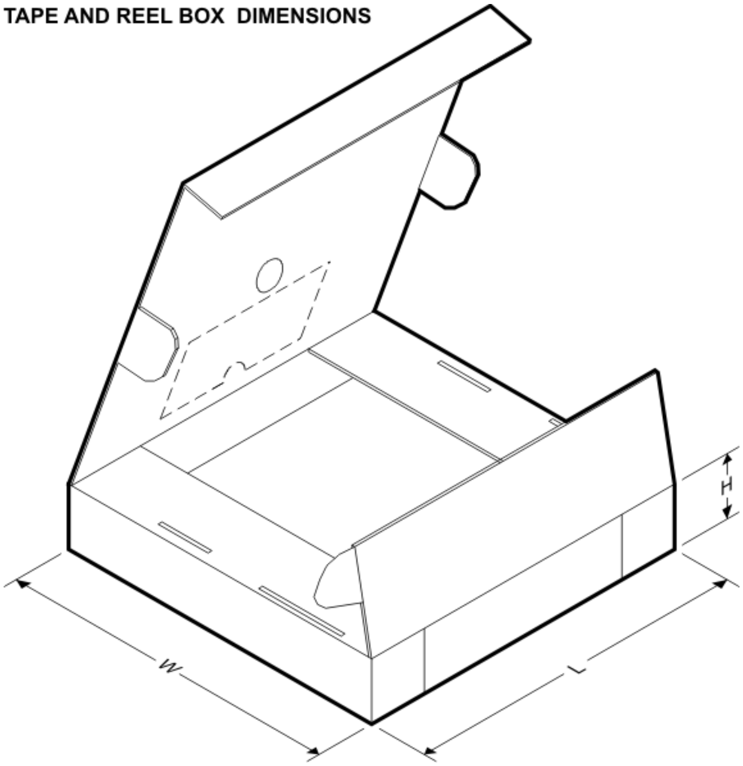
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA212AQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AQDCKRQ1	SC70	DCK	6	3000	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA213AQDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA214AQDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

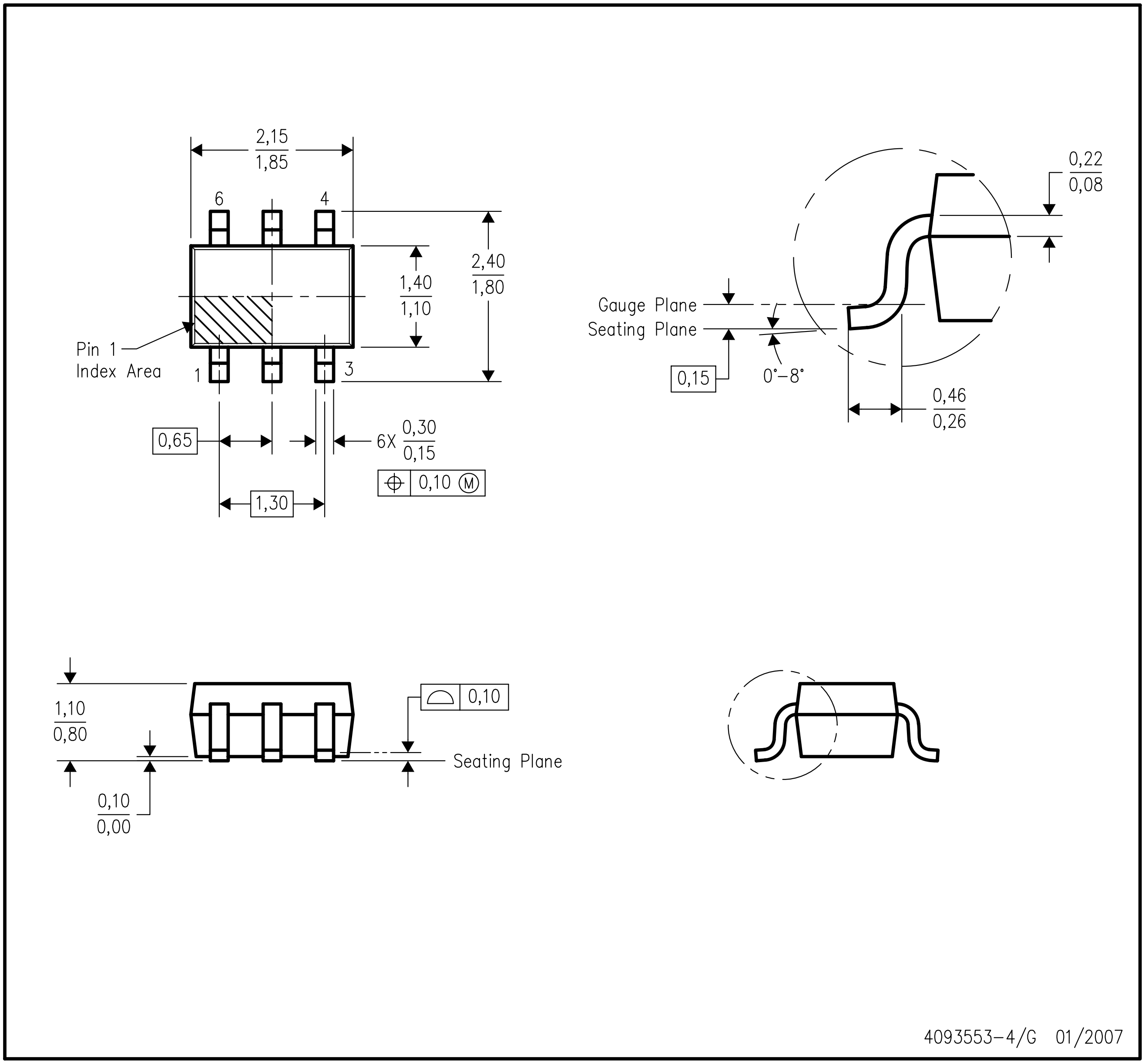
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

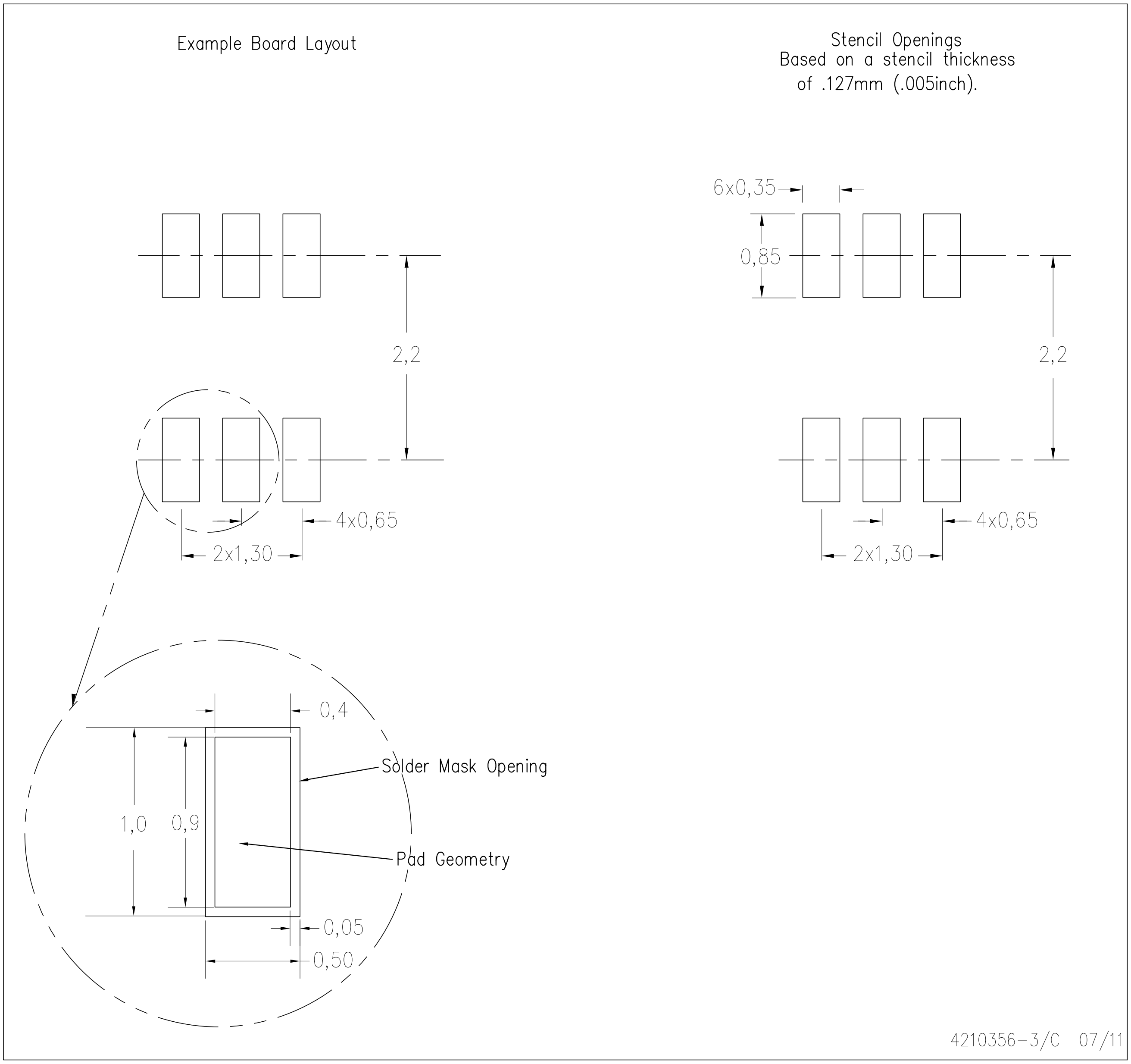
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA212AQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA213AQDCKRQ1	SC70	DCK	6	3000	340.0	340.0	38.0
INA213AQDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0
INA214AQDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

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