Compact PMU with 3 Channels of 3.5A Fast Response, Adaptive COT Bucks

DESCRIPTION

The ETA9351 is a Power Management Unit (PMU) with 3 channels of high frequency synchronous Step-Down converters. Each channel is capable of delivering up to 3.5A output current and accepts input voltage from 2.6V to 5.5V. Each channel has an adaptive Constant-On-Time control scheme that achieves fast transient response while maintaining a constant switching frequency. It does not have the minimum on-time constrain normally a fixed-frequency current mode Step-down requires. Each channel can be independently turned ON/OFF by an enable pin providing flexibility for easy start-up sequencing. All three channel are packed into a small QFN4X4-24L package greatly saving board space.

ETA9351 is available in a tiny QFN4X4-24L package

FEATURES

- Adaptive COT control
- Independent ON/OFF control
- Up to 95% Efficiency
- Up to 91% Efficiency for low output voltage
- Up to 3.5A Max Output current
- Feedback voltage 0.45V
- Excellent load transient response
- QFN4X4-24L Package

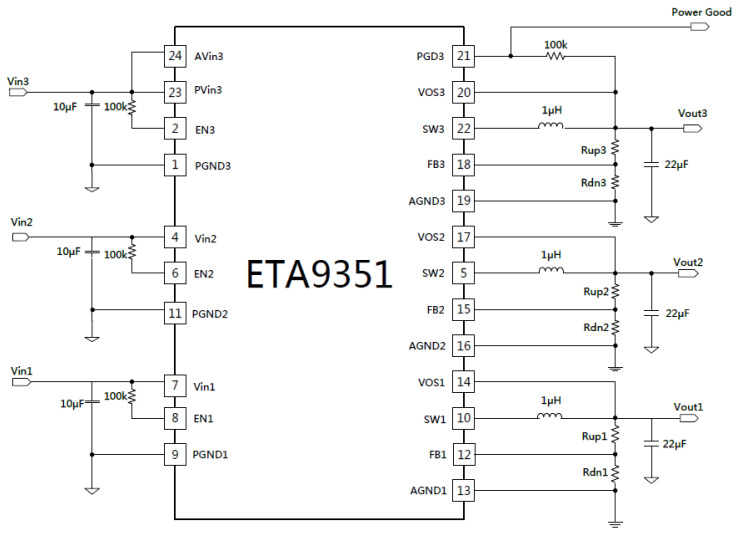
APPLICATIONS

- Smart TV
- IP CAM
- Security CAM
- Car DVR
- Set Top Boxes
- Solid-State-Disk
- MIDs and Tablet PCs
- Other Battery Powered Devices

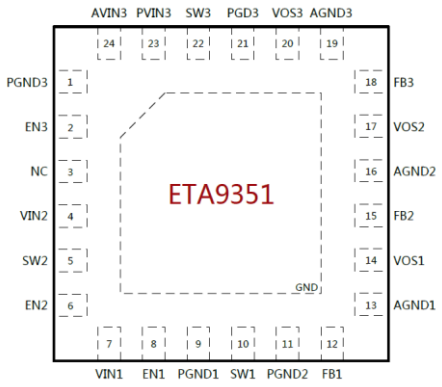
ORDERING INFORMATION

PART	PACKAGE PIN	TOP MARK
ETA9351Q4Y	QFN4x4-24L	ETA9351 YWW2L *- Date Code*

TYPICAL APPLICATION



PIN CONFIGURATION



ABSOLUTEMAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN Voltage .....–0.3V to 6.0V
All Other Pin Voltage .....VIN–0.3V to VIN+0.3
SW to ground current.....Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C
Thermal Resistance θ_{JA}
QFN4x4-24.....30 ..... °C/W
Lead Temperature (Soldering, 10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD MM (Machine Mode) 200V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C. Single Channel)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
General Characteristics for each Channel					
Input Voltage Range		2.6		5.5	V
Input UVLO	Rising, Hysteresis=250mV		2.15		V
Input OVP	Rising, Hysteresis=200mV		6.25		V
Input Supply Current	V_{FB} =0.5V, Device Not Switching		50		μA
Input Shutdown Current	EN=GND		0.1	1	μA
FB Feedback Voltage		0.436	0.45	0.464	V
FB Input Current			0.01		μA
Output Voltage Range		0.45		V_{IN}	V
Load Regulation	V_{IN} =4V, I_{OUT} =0.01A to 3.5A		0.5		%/A
Line Regulation	V_{IN} =3V to 4V, I_{OUT} =1A		0.1		%/V
Switching Frequency		1.0	1.5	2.0	MHz
PMOS Switch On Resistance	I_{SW} =200mA		120		mΩ
NMOS Switch On Resistance	I_{SW} =200mA		60		mΩ
PMOS Switch Current Limit	Vin=5V	4	4.5		A
SW Leakage Current	V_{IN}=5.5V,V_{SW}=0 or 5.5V,EN=GND			10	μA
EN Input Current				1	μA
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.5			V
Thermal Shutdown	Rising, Hysteresis =20°C		155		°C
Power Good (only for Channel 3)					
Power Good Threshold	Rising, Hysteresis=2.5%		90		%
Power Good Low level	$I_{(SINK)}$=1mA			0.4	V

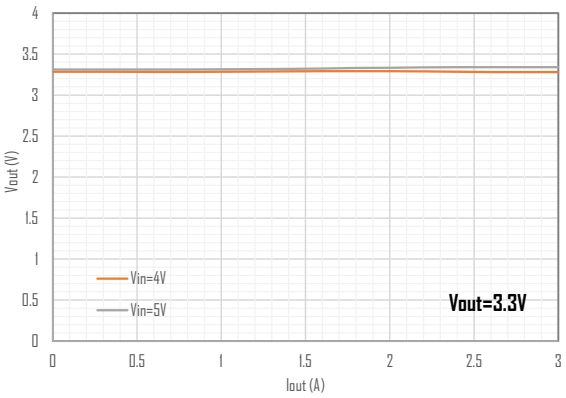
PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	PGND3	Power Ground for channel 3.
2	EN3	Enable pin for the Channel 3. Drive this pin to high to enable channel 3, low to disable.
3	PGND2	Power Ground for channel 2.
4	VIN2	Input Supply Voltage for Channel 2. Bypass with a 22μF ceramic capacitor to PGND2 and 10nF to AGND2.
5	SW2	Inductor Connection for Channel 2. Connect an 1uH inductor Between SW2 and VOS2 output
6	EN2	Enable pin for the Channel 2. Drive this pin to high to enable channel 2, low to disable.
7	VIN1	Input Supply Voltage for Channel 1. Bypass with a 22μF ceramic capacitor to PGND1 and 10nF to AGND1.
8	EN1	Enable pin for the Channel 1. Drive this pin to high to enable channel 1, low to disable.
9	PGND1	Power Ground for channel 1.
10	SW1	Inductor Connection for Channel 1. Connect an 1uH inductor Between SW1 and VOS1 output
11	PGND2	Power Ground for Channel 2.
12	FB1	Feedback Input for Channel 1. Connect an external resistor divider from the output to FB1 and AGND1 to set the output to a voltage between 0.45V and VIN1
13	AGND1	Analog Ground for Channel 1. To keep this ground free from noise by connecting a 10nF ceramic capacitor to VIN1
14	VOS1	Output voltage sense pin for Channel 1, to be connected to the output node of regulator.
15	FB2	Feedback Input for Channel 2. Connect an external resistor divider from the output to FB2 and AGND2 to set the output to a voltage between 0.45V and VIN2
16	AGND2	Analog Ground for Channel 2. To keep this ground free from noise by connecting a 10nF ceramic capacitor to VIN2
17	VOS2	Output voltage sense pin for Channel 2, to be connected to the output node of regulator.
18	FB3	Feedback Input for Channel 3. Connect an external resistor divider from the output to FB3 and AGND3 to set the output to a voltage between 0.45V and VIN3
19	AGND3	Analog Ground for Channel 3. To keep this ground free from noise by connecting a 10nF ceramic capacitor to VIN3
20	VOS3	Output voltage sense pin for Channel 3, to be connected to the output node of regulator.
21	PG3	Power Good Pin for Channel 3. This pin is high impedance if the output voltage is within regulation. This pin is pulled low if the output is below its nominal value. The pull up resistor cannot be connected to any voltage higher than voltage of VIN3
22	SW3	Inductor Connection for Channel 3. Connect an 1uH inductor Between SW3 and VOS3 output
23 24	PVIN3 AVIN3	Input Supply Voltage for Channel 1. Bypass with a 22μF ceramic capacitor to PGND3 and 10nF to AGND3.

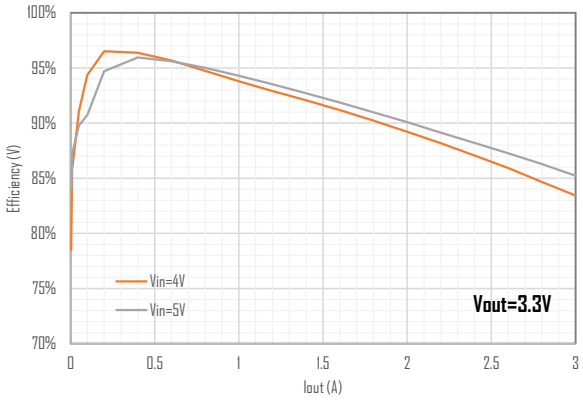
TYPICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified for single channel.)

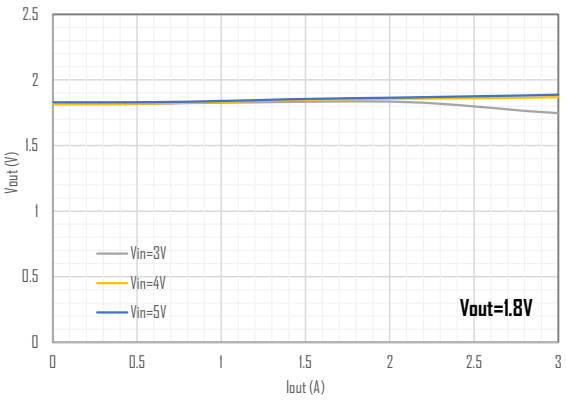
Vout Vs. Iout



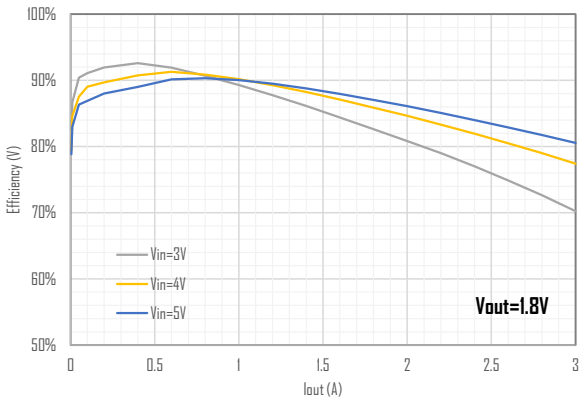
Efficiency Vs. Iout



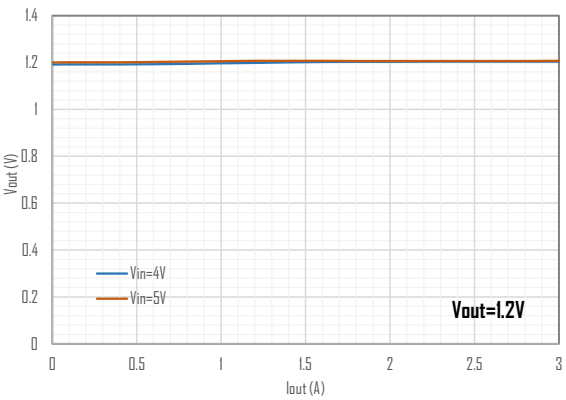
Vout Vs. Iout



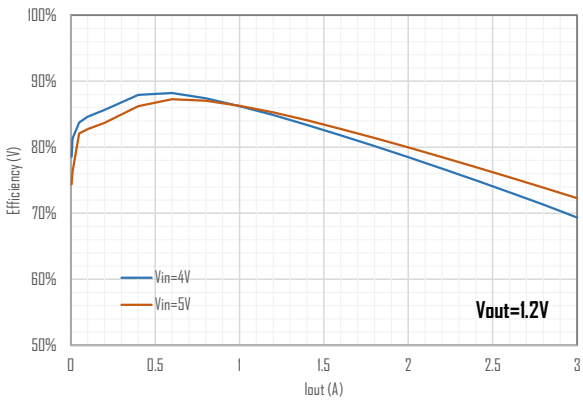
Efficiency Vs. Iout



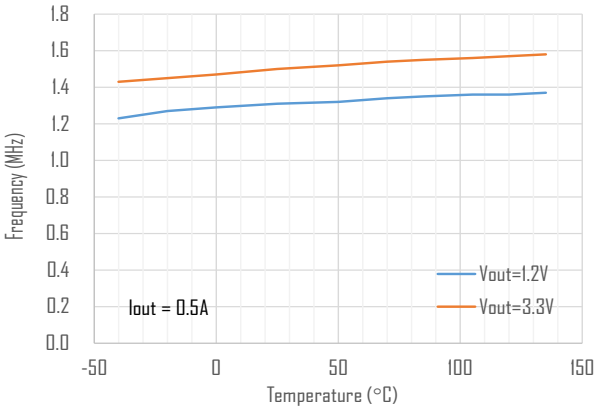
Vout Vs. Iout



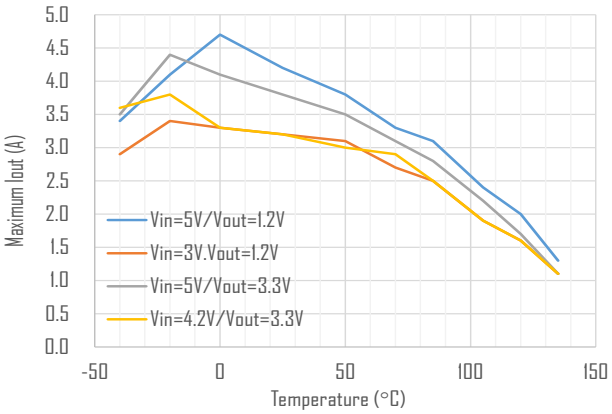
Efficiency Vs. Iout



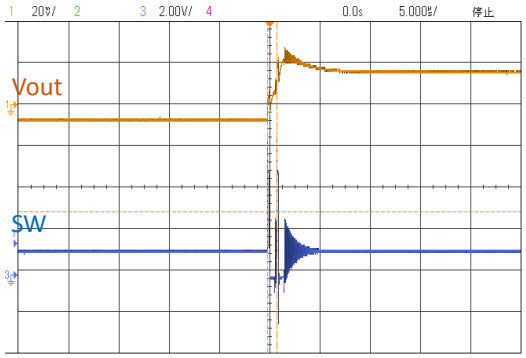
Switching Frequency Vs. Ambient Temperature



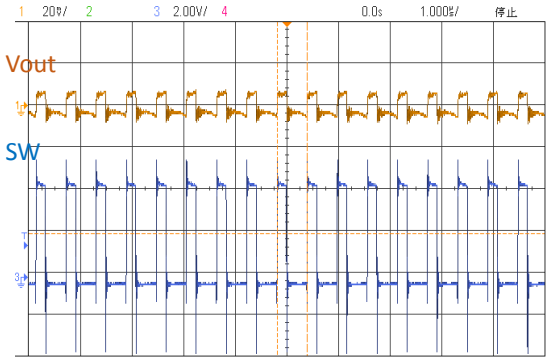
Maximum Iout Vs. Ambient Temperature



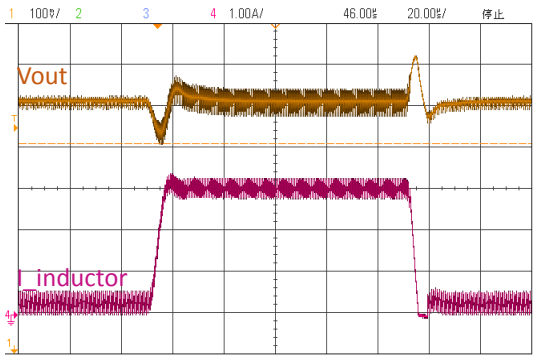
Switching Waveform: V_{IN}=5V, Vout=1.2V, I_{OUT}=0 mA



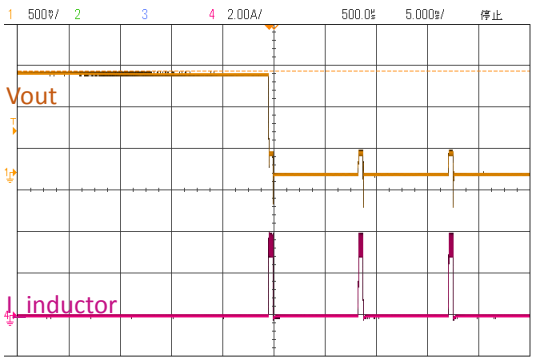
Switching Waveform: V_{IN}=5V, Vout=1.2V, I_{OUT}= 3A



Transient Response: V_{IN}=5V, Vout=1.2V, I_{OUT}=0.3 - 3A



Output Short Response: V_{IN}=5V, Vout=1.2V, Output short to GND



FUNCTIONAL DECRIPTIONS for each channel

The ETA9351 is a Power Management Unit (PMU) with 3 channels of high frequency synchronous Step-Down converters. Each channel combines the advantages of voltage mode control and Constant On time control. Its adaptive Constant-On-Time control dynamically changes switch on time to achieve a constant switching frequency. It does not have the minimum on-time constrain normally a fixed-frequency current mode Step-down requires, allowing it to go down to very low duty ratios without affecting loop stability. The voltage mode nature of each channel also provides a more superior load transient response as well as a seamless transition from PFM to PWM modes. It can also operate up to 100% duty. It has a cycle by cycle current limit and a hiccup mode that protects against dead-short condition. It includes soft-start, UVLO and thermal shutdown protection.

Adaptive Constant On-Time Control

ETA9351 uses an adaptive Constant-On-Time control scheme that the ON time is dynamically adjusted according to VIN and VOUT so to achieve a nearly constant switching frequency. This control scheme provides simpler compensation and superior transient response over traditional constant frequency current mode control, while still maintaining the advantage of switching at a constant frequency at about 1.5MHz. It also provides a seamless transition from PFM to PWM that normally a constant frequency current mode control scheme is hard to achieve. Further mode, because it is a COT control scheme, the system can achieve high step-down ratio at ease, because lower constrain on the minimum on- time requirement existing in constant frequency scheme.

100% Duty operation

ETA9351 can operate at 100% duty cycle under dropout condition for high efficiency purpose.

Current Limit and Short-Circuit protection

ETA9351 employs a cycle-by-cycle peak current limit and it also has a hiccup mode that protects the circuit during dead-short condition. When the dead-short condition is removed, the IC goes back to normal operation.

Soft-start

ETA9351 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If IN drops below UVLO threshold, the UVLO circuit inhibits switching. Once IN rises above ULVO threshold, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J= +155°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Design Procedure for each channel

Setting Output Voltages

Output voltages are set by external resistors. The FB threshold is 0.45V.

$R_{TOP} = R_{BOTTOM} \times [(V_{OUT} / 0.45) - 1]$

Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum overcurrent trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. $L_{IDEAL}=(V_{IN(MAX)}-V_{OUT})/I_{RIPPLE}*D_{MIN}*(1/F_{OSC})$

Output Capacitor Selection

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, or a MLCC capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$V_{RIPPLE} = IL_{(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE(ESR)} = IL_{(PEAK)} \times ESR$

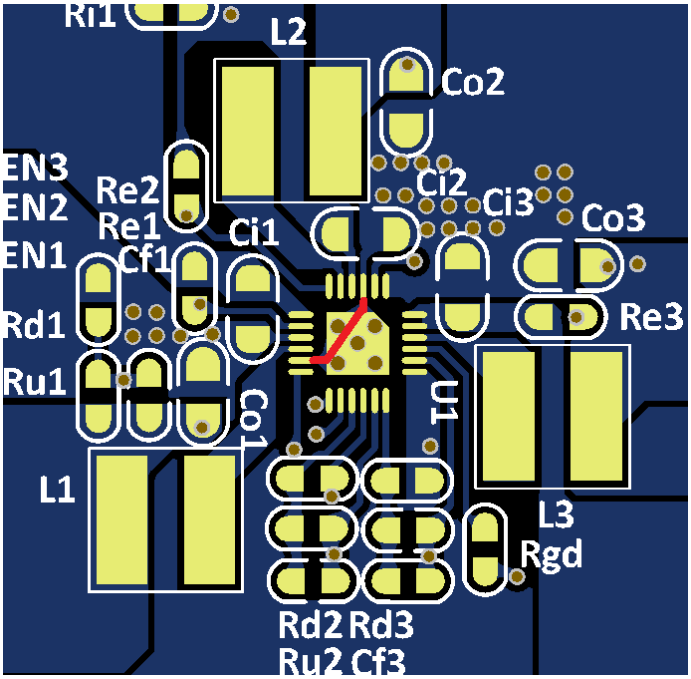
Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability.

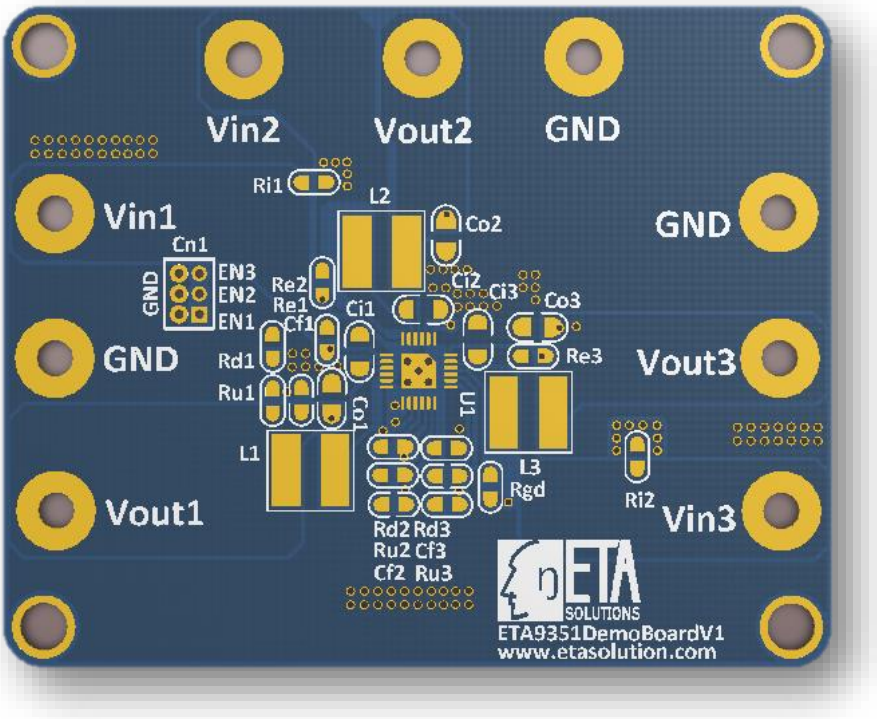
PCB LAYOUT Guide

The ETA9351 employs a sophisticated control scheme to achieve the fast response and other superior performances. So the PCB layout is recommended to strictly follow the proposed way shown below. The Cin (10uF) and Cout (22uF or 10uF x 2) are always to be placed closest to ETA9351.

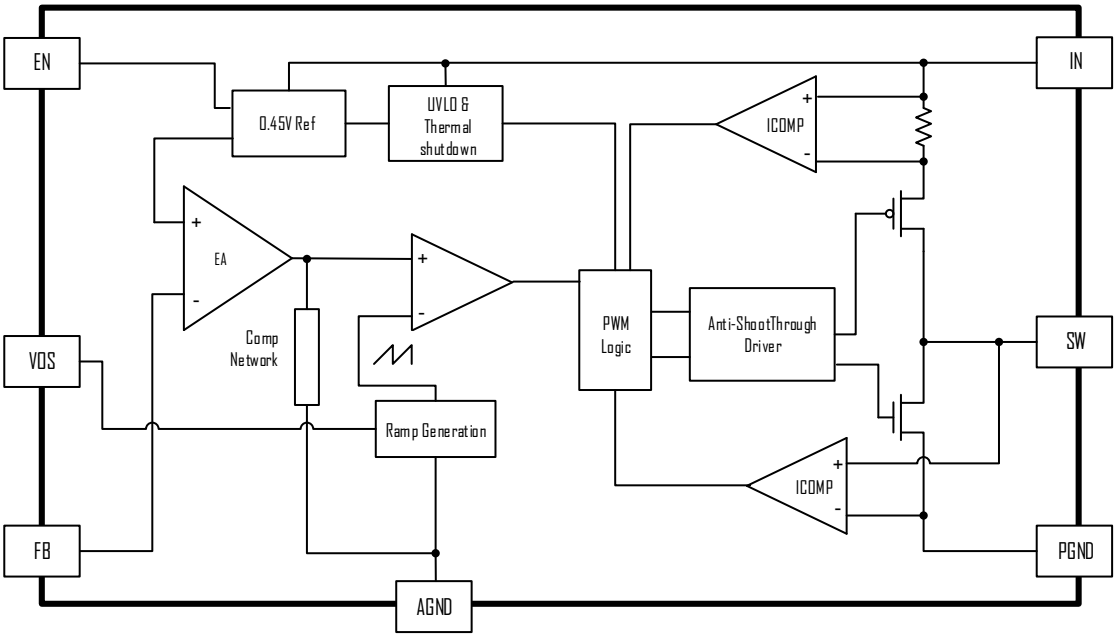
Please follow the example of PCB layout which is shown below to place the important input capacitors of each channel. And also please be aware of the PGND trace of Channel 2, wiring PGND2 of Pin11 through bottom heat dissipation plate to Pin3 (the NC pin) to enable the Ci2 (input capacitor of Channel 2) to have the shortest power path connecting. The wire is demonstrated in red line below.



A complete view of ETA9351 demo board is attached hereafter for reference.

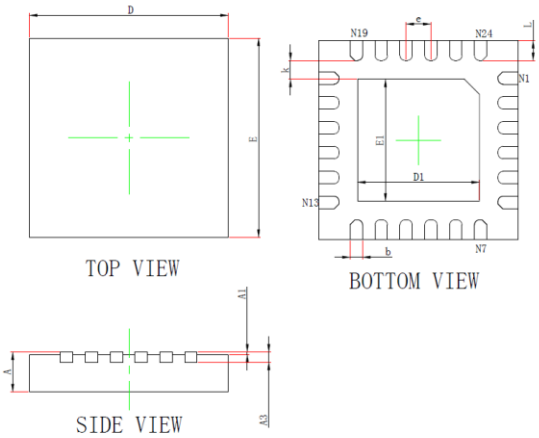


BLOCK DIAGRAM for ONE CHANNEL



PACKAGE OUTLINE

Package: QFN4X4-24L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.950	4.050	0.156	0.159
E	3.950	4.050	0.156	0.159
E1	2.400	2.500	0.094	0.098
D1	2.400	2.500	0.094	0.098
k	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.350	0.450	0.014	0.018