

DESCRIPTION

The MT3033 is a 3A high frequency synchronous Step-Down converter using constant frequency, current mode architecture. The device integrates main switch and synchronous rectifier switch for high efficiency without an external schottky diode. To maximize light load efficiency, The MT3033 draws only 40µA quiescent current to improve light load efficiency. In shutdown, The MT3033 reduces supply current less than 1µA. The MT3033 can supply 3A of load current from 2.5V to 6.0V input voltage. The output voltage can be regulated as low as 0.6V. The switching frequency is internally set at 1MHz. The MT3033 automatically operates PSM or PWM mode depending on the external load. The MT3033 has built-in internal Soft Start, Short Circuit Protection and Thermal shutdown functions, allowing the use of small surface mount inductors and capacitor. The MT3033 is available in a low profile DFN3x3_10L package.

FEATURES

- Input Voltage Range from 2.5V to 6.0V
- +/- 2% 0.6V Feedback Voltage Accuracy
- 1MHz Switching Frequency
- Continuous Output Current up to 3A
- Low Quiescent Current of 40µA
- Power Good Indicator
- 0.1µA Shutdown Current
- 100% Duty Cycle Operation
- Built-in 110/80mΩ Power Switch
- Internal Soft-Start
- Cycle-by-Cycle Current Limit Protection
- Over-Load and Hiccup Mode Short Circuit
- Thermal Shutdown Protection
- PWM with Power Saving Mode
- Available in a Small DFN3x3mm_10L Package
- Pb-Free RoHS Compliant

APPLICATIONS

- Solid-State and Hard Disk Drives
- Wireless and DSL Card
- Portable/Handheld Device
- STB, TV, Sound Bar, MP3 Player
- Microprocessor and DSP Core Supply



Effciency VIN=5V



Typical Applications





Ordering Information

Part No.	Marking	Temp. Range	Package	MOQ
MT3033NDCR	MT3033 YWWxx	-40°C ~+85°C	DFN3x3_10L	5000/Tape & Reel

Note: Y:Year, WW:Week

Pin Configuration



Pin Description

Pin No.	Symbol	Description
1, 2, 3	SW	Power Switches Node
4	PG	Open-Drain Power Good Indicator. Connect a $100k\Omega$ pull-up resistor to VIN. This pin is high impedance if the output voltage is within regulation. It is pulled low if the output is below its nominal value. Leave the pin float if no used.
5	EN	Regulator Enable Control Input, Don't float this PIN Drive EN above 1.2V to turn on the converter Drive EN below 0.3V to turn off the converter
6	FB	Output Voltage Feedback Input. Connect to the external feedback resistors.
7	NC	Not Connected
8	SVIN	Signal Power Input Supply Voltage
9, 10	PVIN	Power Input Supply Voltage, Decouple this pin to GND with at least 22µF ceramic cap.
EP	GND	Power Ground



Absolute Maximum Rating (Reference to GND) (Note1)

Input Supply Voltage GND-0.3V to +6V	Jun
EN, FB Voltage0.3V to 6V	Stor
ESD Classification Class 2	Lea

unction Temperature Range40°C to 150°C	
Storage Temperature Range65°C to 150°C	
ead Temperature (Soldering 10s) 260°C	

Thermal Resistance (θ_{JC}) 8.2°C/W

Recommend Operating Conditions (Note2)

Input Voltage (V _{IN}) +2.5V to +6V	Operating Temperature Range40°C to +85°C
Thermal information (Note3)	
Maximum Power Dissipation(TA=+25°C) 1.8W	Thermal Resistance (θ_{JA})

Note (1): Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside of the recommended operating conditions.

Note (3): Measured on JESD51-7, 4-Layer PCB.

Note (4): The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX} , the junction to ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_{D_MAX} = $(T_{J_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Functional Block Diagram





Electrical Characteristics

 $T_A = 25^{\circ}C$, $V_{IN}=5V$, unless otherwise noted.

PARAMETER	TEST CONTITIONS	MIN	TYP	MAX	UNIT
Input Supply Voltage		2.5		6.0	V
Quiescent Current	$V_{EN} = V_{IN}, V_{FB} = 0.65V,$ I_{OUT} =0A, No switching		40	60	μA
Shutdown Current	$V_{EN} = 0V$		0.1	1.2	μΑ
Regulated Feedback Voltage V_{REF}	$T_A = 25^{\circ}C$	0.588	0.6	0.612	V
Feedback Current		-30		30	nA
VIN Under voltage	VIN rising		2.2		V
Lockout Threshold	VIN falling		1.9		v
PMOSFET On Resistance	$I_{SW} = 100 \text{mA}$, $V_{IN} = 5 \text{V}$		110		mΩ
NMOSFET On Resistance	I_{SW} = -100mA , V_{IN} =5V		80		mΩ
PMOSFET Current Limit	V _{IN} =3.3V		5		А
SW Leakage Current	$V_{EN} = 0V, V_{IN} = 6.0V$ $V_{SW} = 0V \text{ or } 6.0V$	-1		1	μA
Oscillator Frequency	I _{OUT} =1A		1		MHz
Min. On-Time for HS Switch			100		ns
Maximum Duty	V _{FB} < 0.6V			100	%
EN On Threshold		1.5			V
EN Off Threshold				0.4	V
EN Pull-up Current	$V_{EN} = 0V$		0.8	3	μA
Power Good Indication	Vout falling with respect to Vout Nominal Value		90		%
Power Good Pull Low	VFB=0.5V, Isink=1mA		0.1	0.3	V
Soft Start Time			0.76		ms
Thermal Shutdown Threshold			160		°C



TYPICAL PERFORMANCE CHARACTERISTICS

(CIN=22uF, COUT = 44uF, L=2.2uH, TA=25 $^{\circ}$ C)





















TYPICAL PERFORMANCE CHARACTERISTICS

 $(C_{IN}=10uF, C_{OUT}=22, L=2.2uH, T_{A}=25$ °C)











Detailed Description

The MT3033, a current mode PWM step-down converter with a constant frequency, is optimized for low voltage, Lilon battery powered applications for which the high efficiency and small size are critical. It uses an external resistor divider to set the output voltage from 0.6V to Vin and integrates both a main switch and a synchronous rectifier, which provides the high efficiency and eliminates an external Schottky diode. MT3033 has power saving mode to provide high efficiency at light load.

Current Mode PWM Control

Current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load and line response and protection of the internal main switch and synchronous rectifier. The MT3033 switches at a constant frequency (1MHz) and regulates the output voltage.

During normal operation, the hidden side is turned on at the beginning of a clock cycle when the VFB voltage is below the Vref (0.6V). The current flows into the inductor and the load increases until the current limit is reached. The switch is turned off and energy stored in the inductor flows through the low side switch into the load until the next clock cycle.

Power Saving Mode

The power saving mode at light load can minimize the switching loss by reducing the switching frequency. Therefore, the MT3033 is designed as the power saving mode for high efficiency at light load.

Under Voltage Lockout

The MT3033 features an Under-Voltage Lockout circuit, which provides the function to shut down the part when the input voltage drops below about 2.10V to prevent unstable operation.

Internal Soft-start

The MT3033 features an internal soft–start function, which reduces inrush current and overshoot of the output voltage. Soft–start is achieved by ramping up the reference voltage (V_{ref}) which is applied to the input of the error amplifier. The typical soft–start time, depending on the component's values on AP circuit, is about 650µsec.

Short Circuit Protection

The MT3033 has short circuit protection. When the output is shorted to ground, the oscillator's frequency is reduced to prevent the inductor's current from increasing beyond the P MOSFET current limit. The frequency will return to the normal values once the short circuit condition is removed and the feedback voltage > 0.3V.

Maximum Load Current

The MT3033 can operate down to 2.5V input voltage; however the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the inductor's peak current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the decrease of the duty cycle matches other diagrams in this datasheet.



Application Information

Input Capacitor Selection

It is necessary for the input capacitor to sustain the ripple current produced during the period of "ON" state of the upper MOSFET, so a low ESR is required to minimize the loss. The RMS value of this ripple can be obtained by the following:

$$I_{\text{INRMS}} = I_{\text{OUT}} \sqrt{D \times (1 - D)}$$

Where D is the duty cycle, I_{INRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. The loss of the input capacitor can be calculated by the following equation:

$$P_{CIN} = ESR_{CIN} \times I_{INRMS}^2$$

Where P_{CIN} is the power loss of the input capacitor and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large di/dt through the input capacitor, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge-protected. Otherwise, capacitor failure could occur.

Output Inductor Selection

The output inductor selection is to meet the requirements of the output voltage ripple and affects the load transient response. The higher inductance can reduce the inductor's ripple current and induce the lower output ripple voltage. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \bullet \frac{V_{OUT}}{V_{IN}}$$
$$\Delta V_{OUT} = \Delta I \times ESR$$

Although the increase of the inductance reduces the ripple current and voltage, it contributes to the decrease of the response time for the regulator to load transient. The way to set a proper inductor value is to have the ripple current (\triangle I) be approximately 20%~50% of the maximum output current. Once the value has been determined, select an inductor capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. 20% tolerance (at room temperature) is reasonable for the most inductor manufacturers. For some types of inductors, especially those with ferrite core, the ripple current will increase abruptly when it saturates, which will result in-a larger output ripple voltage.

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The high capacitor value and low ESR will reduce the output ripple and the load transient drop. In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by the following equations:

$$\mathsf{ESR}_{\mathsf{MAX}} = \frac{\Delta \mathsf{V}_{\mathsf{ESR}}}{\Delta \mathsf{I}_{\mathsf{OUT}}}$$



Number of capacitors = $\frac{\text{ESR}_{\text{CAP}}}{\text{ESR}_{\text{MAX}}}$

 $\triangle V_{ESR}$ = change in output voltage due to ESR $\triangle I_{OUT}$ = load transient ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet) ESR_{MAX} = maximum allowable ESR

High frequency decoupling capacitors should be placed as closely to the power pins of the load as physically possible. For the decoupling requirements, please consult the capacitor manufacturers for confirmation.

Output Voltage

The output voltage is set using the FB pin and a resistor divider connected to the output as shown in AP Circuit below. The output voltage (V_{OUT}) can be calculated according to the voltage of the FB pin (V_{FB}) and ratio of the feedback resistors by the following equation, where (V_{FB}) is 0.6V:

$$V_{FB} = V_{OUT} \times \frac{R_2}{(R_1 + R_2)}$$

Thus the output voltage is:

$$V_{OUT} = 0.6 \times \frac{(R_1 + R_2)}{R_2}$$

Choose R1=100k Ω ~200k Ω to ensure feedback loop noise immunity. It is optional to add a feed-forward capacitor C_{FF}=22~33pF in parallel with R1 to achieve better transient response performance.

Layout Consideration

The physical design of the PCB is the final stage in the design of power converter. If designed improperly, the PCB could radiate excessive EMI and contribute instability to the power converter. Therefore, following the PCB layout guidelines below can ensure better performance of MT3033.

- (1). The loop (Vin-SW-L-Cout-GND) indicates a high current path. The traces within the loop should be kept as wide and short as possible to reduce parasitic inductance and high-frequency loop area. It is also good for efficiency improvement.
- (2). Input capacitor as close as possible to the IC Pins (Vin and GND) and the input loop area should be as small as possible to reduce parasitic inductance, input voltage spike and noise emission.
- (3). Feedback components (R₁, R₂ and C_{FF}) should be routed as far away from the inductor and the SW Pin as possible to minimize noise and EMI issue.
- (4). For a typical 2-layer PCB layout, please refer to EVB Top Layer and EVB Bottom Layer below.



MT3033 Application Schematic



Qty	Ref	Val	ue	Description	Package	
1	CIN	22	١F	Ceramic Capacitor, 10V, X5R	0805	
2	Соит	22	١F	Ceramic Capacitor, 10V, X5R	0805	
1	Cff	22	p	Ceramic Capacitor, 10V, X5R	0603	
1	CEN	0.1	μF	Ceramic Capacitor, 10V, X5R	0603	
1	L1	1µH~2	2.2µH	Inductor, 5A	SMD	
		Vout=3.3V	200ΚΩ			
		Vout=2.5V	187KΩ		0603	
1	R1	R1 Vout=1.8V 200K	R1 Vout=1.8V 200KΩ Resistor, ±1%	Resistor, ±1%		
		Vout=1.2V	100KΩ			
		Vout=1V	66.5KΩ			
		Vout=3.3V	44.2KΩ			
		Vout=2.5V	59KΩ			
1	R2	Vout=1.8V	100KΩ	Resistor, ±1%	0603	
		Vout=1.2V	100KΩ			
	Vout=		100KΩ			
2	Rpg, Ren	100	KΩ	Resistor, ±1%	0603	
1	U1	MT3	033	Step-Down DC/DC Converter	DFN3x3_10L	

EVB BOM List



Package Information

DFN 10L 3x3mm Outline Dimensions

Unit: inches/mm



	MILLIMETERS		INCHES	
STIVIDULS	MIN.	MAX.	MIN.	MAX.
А	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D1	2.5	0	0.09	8
E	2.90	3.10	0.114	0.122
E1	1.60		0.06	53
е	0.50		0.02	20
L	0.30	0.50	0.012	0.020



Carrier Tape & Reel Dimensions

1. Orientation / Carrier Tape Information :



2. Rokreel Information :



3. Dimension Details :

PKG Type	А	В	С	D	E	F	Q'ty/Reel
Q(D)FN 3x3	4.0 mm	1.5 mm	12.0 mm	8.0 mm	13 inches	13.0 mm	5,000



Reflow Profile

Classification Of IR Reflow Profile

Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts _{min} to Tp)	1~2°C/second, 3°C/second max.
Preheat & Soak	
-Temperature Min(Ts _{min})	150 ℃
-Temperature Max(Ts _{max})	200 ℃
-Time(ts _{min} to ts ts _{max})	60~120 seconds
Time maintained above:	
-Temperature(TL)	217 ℃
-Time(t∟)	60~150 seconds
Peak Temperature(Tp)	See Classification Temp in table 1
Time within 5 $^\circ \! \mathbb{C}$ of actual Peak Temperature(tp)	30 seconds max.
Ramp-Down Rate	6℃/second max.
Time 25 $^\circ\!\!\mathbb{C}$ to Peak Temperature	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. Pb-free Process – Classification Temperatures (Tc	.)
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Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 ℃	260 ℃
1.6 mm – 2.5 mm	260 °C	250 ℃	245 ℃
2.5 mm	250 ℃	245 ℃	245 ℃

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.

