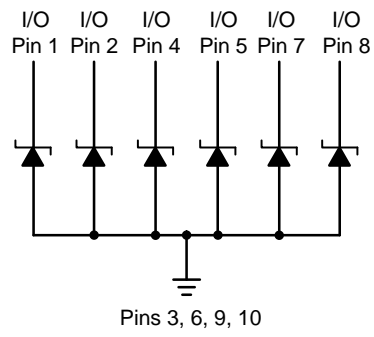


ESD8006



Note: Common GND – Only Minimum of 1 GND connection required

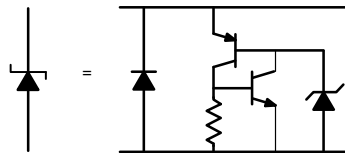
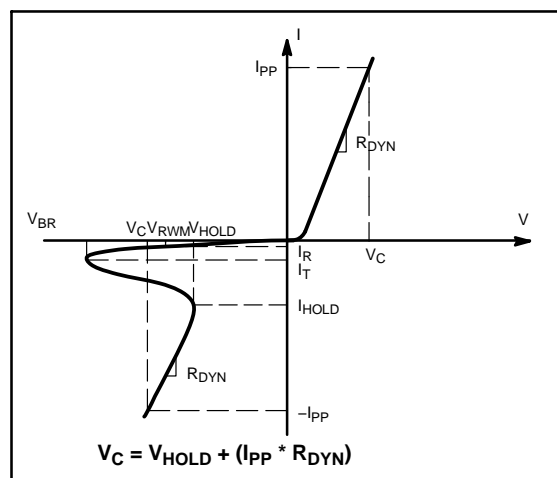


Figure 1. Pin Schematic

ELECTRICAL CHARACTERISTICS(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V _{RWM}	Working Peak Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
V _{HOLD}	Holding Reverse Voltage
I _{HOLD}	Holding Reverse Current
R _{DYN}	Dynamic Resistance
I _{PP}	Maximum Peak Pulse Current
V _C	Clamping Voltage @ I _{PP} V _C = V _{HOLD} + (I _{PP} * R _{DYN})

**ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V _{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V _{BR}	I _T = 1 mA, I/O Pin to GND	5.5	7.0		V
Reverse Leakage Current	I _R	V _{RWM} = 3.3 V, I/O Pin to GND			1.0	μA
Holding Reverse Voltage	V _{HOLD}	I/O Pin to GND		1.19		V
Holding Reverse Current	I _{HOLD}	I/O Pin to GND		25		mA
Clamping Voltage (Note 1)	V _C	IEC61000-4-2, ±8 kV Contact	See Figures 2 and 3			V
Clamping Voltage TLP (Note 2) See Figures 6 through 9	V _C	I _{PP} = 8 A I _{PP} = -8 A } IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		4.9 -5.0		V
		I _{PP} = 16 A I _{PP} = -16 A } IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)		8.4 -9.5		V
Dynamic Resistance	R _{DYN}	I/O Pin to GND GND to I/O Pin		0.44 0.49		Ω
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz between I/O Pins and GND V _R = 0 V, f = 2.5 GHz between I/O Pins and GND V _R = 0 V, f = 5.0 GHz between I/O Pins and GND V _R = 0 V, f = 1 MHz, between I/O Pins			0.32 0.25 0.25 0.16	pF

- For test procedure see Figures 4 and 5 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t₁ = 30 ns to t₂ = 60 ns.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

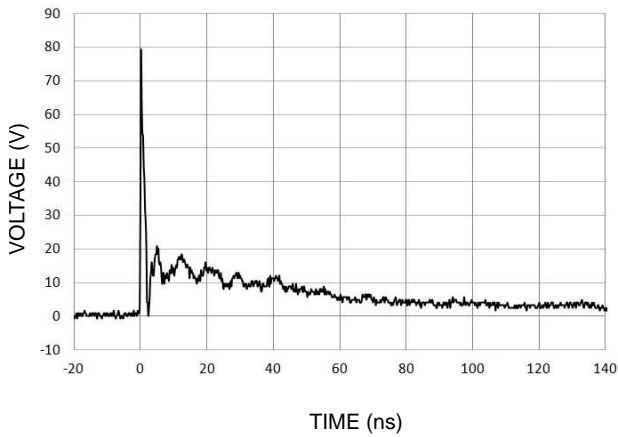


Figure 2. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

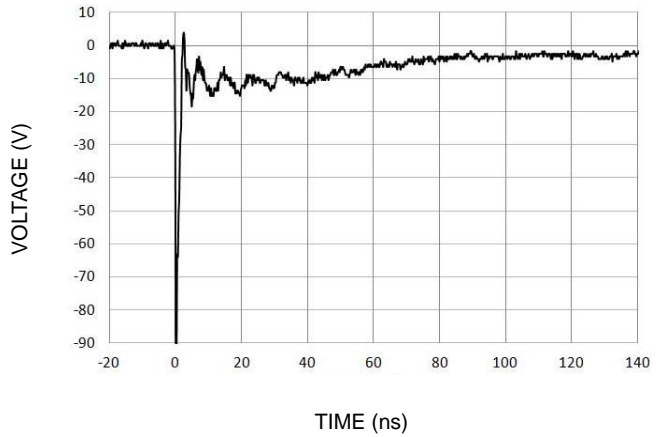


Figure 3. IEC61000-4-2 -8 kV Contact Clamping Voltage

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

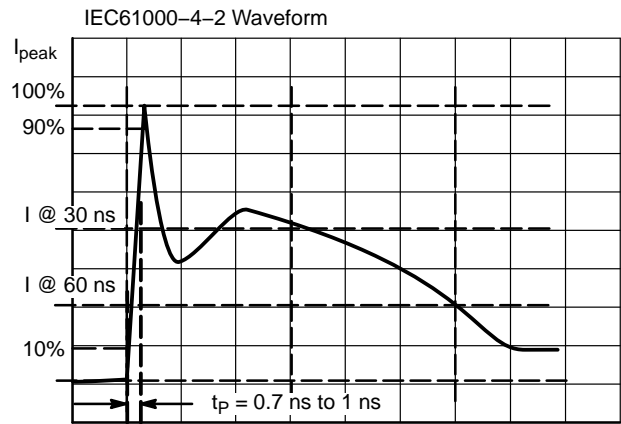


Figure 4. IEC61000-4-2 Spec

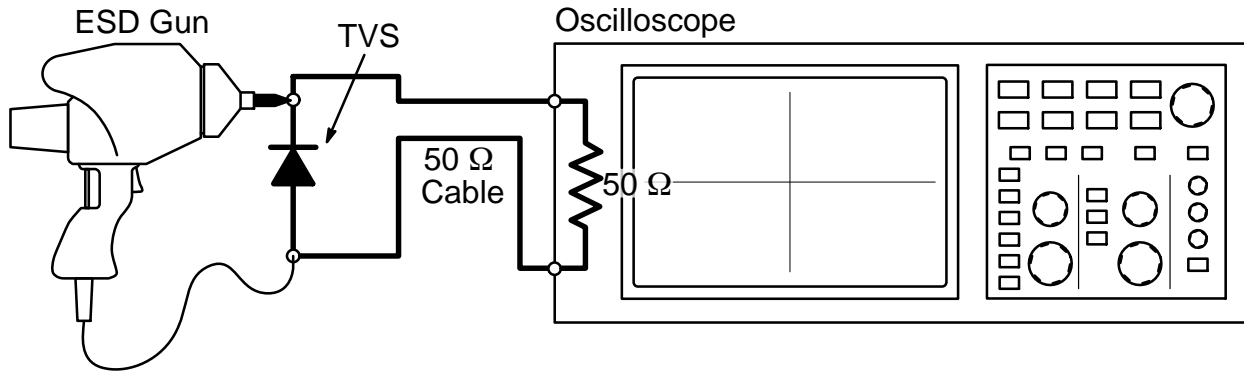


Figure 5. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D – Characterization of ESD Clamping Performance.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D and AND8308/D.

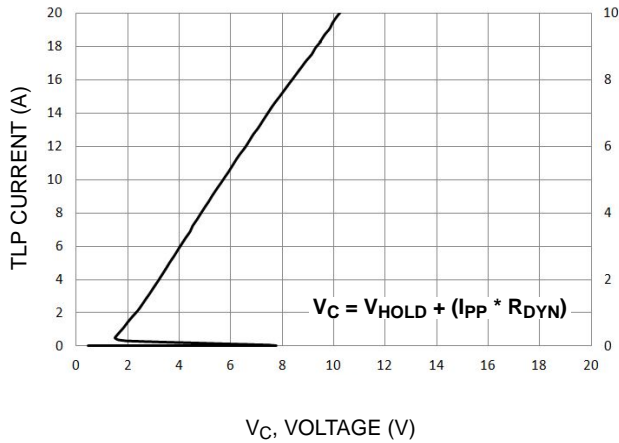


Figure 6. Positive TLP I-V Curve

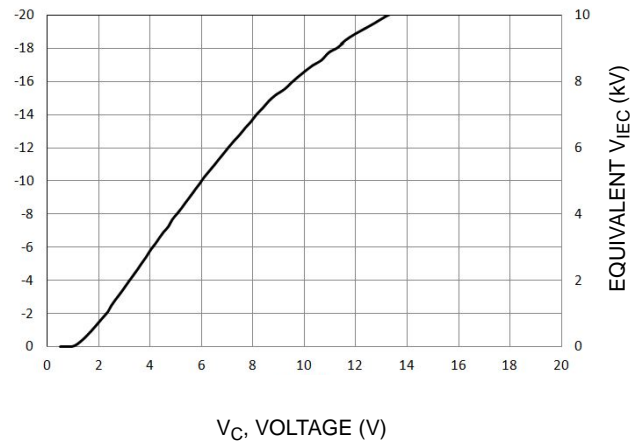


Figure 7. Negative TLP I-V Curve

NOTE: TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 300 \text{ ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000-4-2 waveform at $t = 30 \text{ ns}$ with 2 A/kV . See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

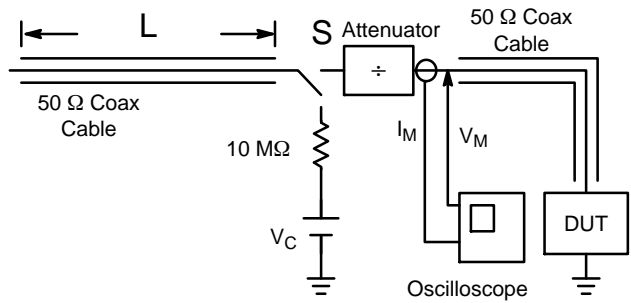


Figure 8. Simplified Schematic of a Typical TLP System

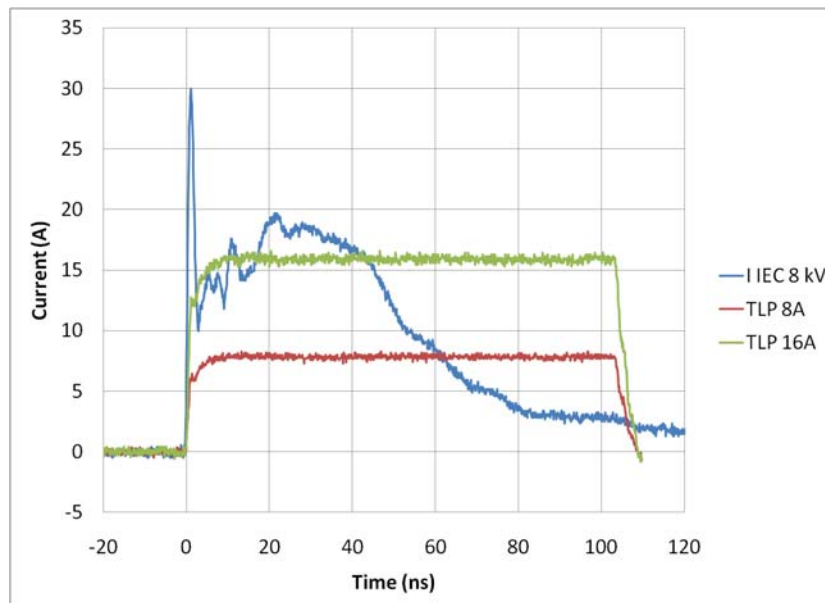


Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

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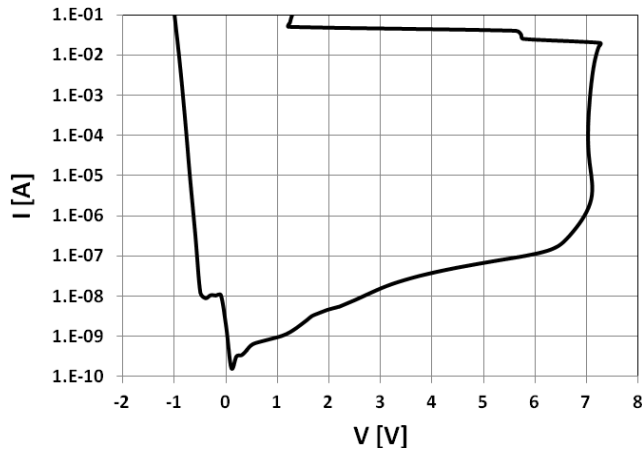


Figure 10. IV Characteristics

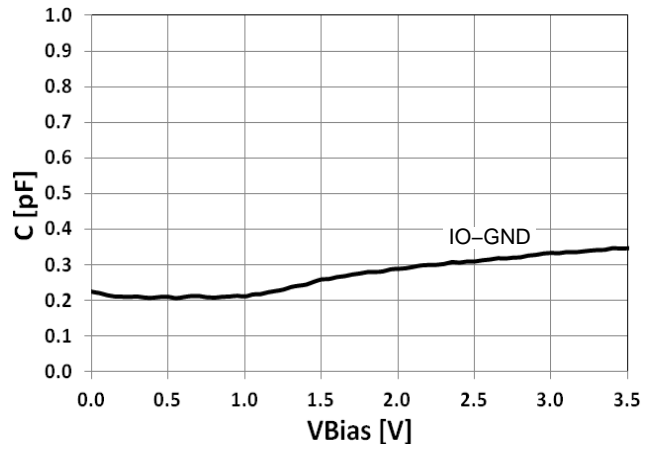


Figure 11. CV Characteristics

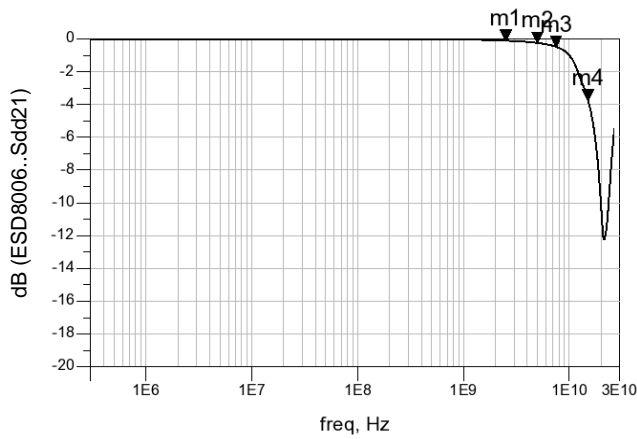


Figure 12. RF Insertion Loss

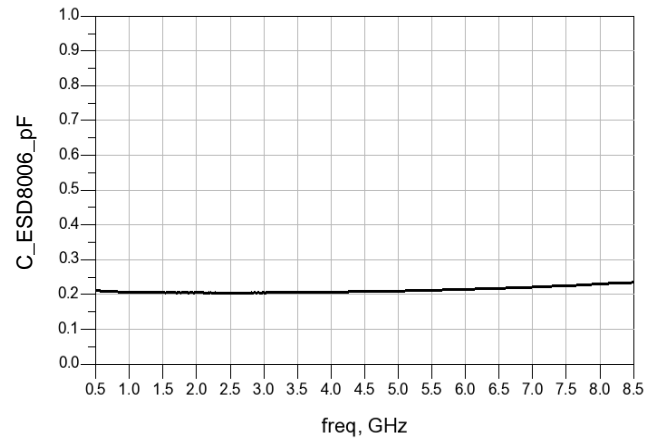


Figure 13. Capacitance over Frequency

TABLE 1. RF Insertion Loss: Application Description

Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	3 rd Harmonic Frequency (GHz)	ESD8006 Insertion Loss (dB)
USB 3.0	5.0	2.5 (m1)	7.5 (m3)	m1 = 0.098 m2 = 0.240 m3 = 0.479 m4 = 3.732
Thunderbolt, USB 3.1	10	5.0 (m2)	15 (m4)	

ESD8006

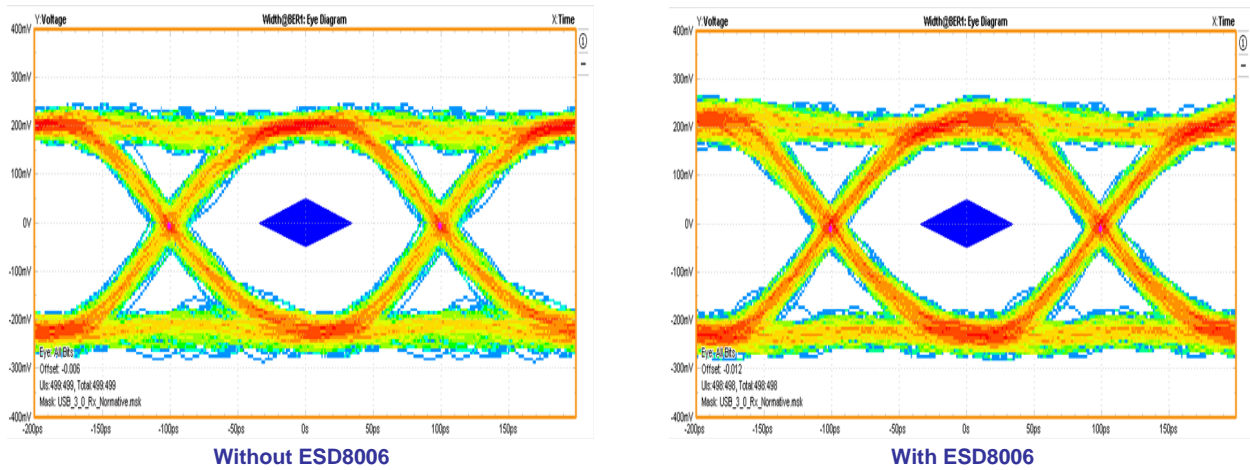


Figure 14. USB 3.0 Eye Diagram with and without ESD8006. 5 Gb/s

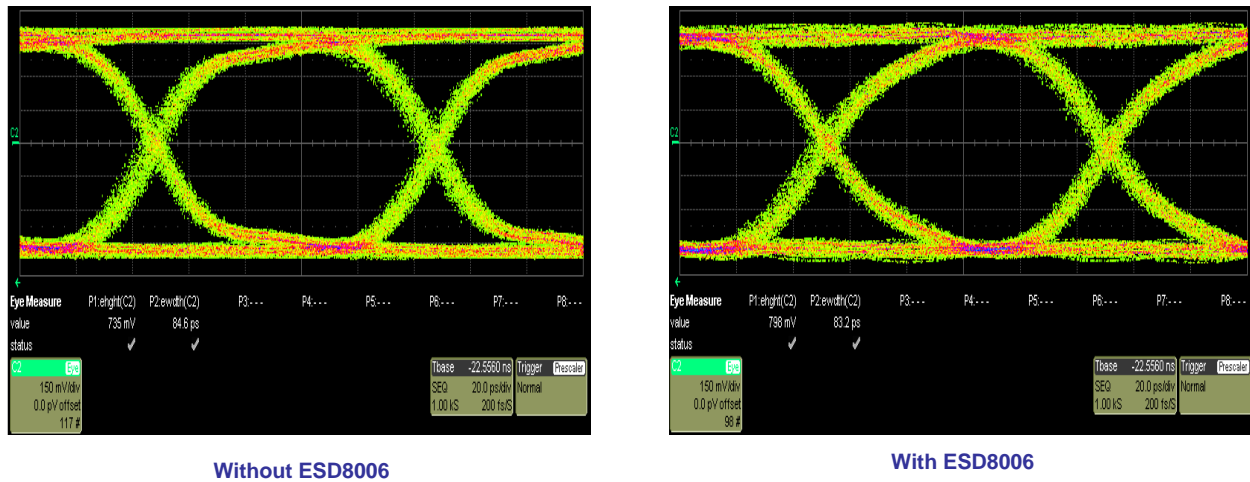


Figure 15. Thunderbolt and USB 3.1 Eye Diagram with and without ESD8006. 10 Gb/s

See application note AND9075/D for further description of eye diagram testing methodology.

ESD8006

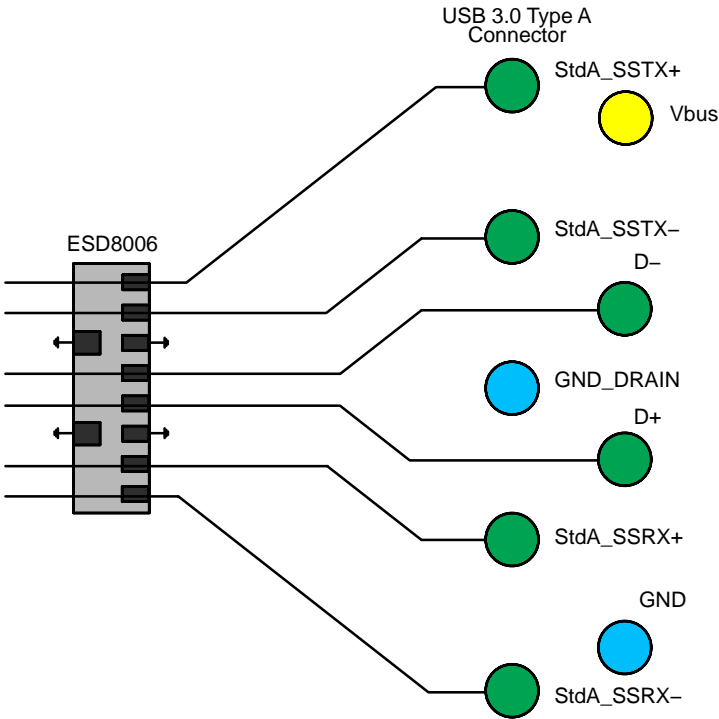


Figure 16. USB 3.0/3.1 Layout Diagram

ESD8006

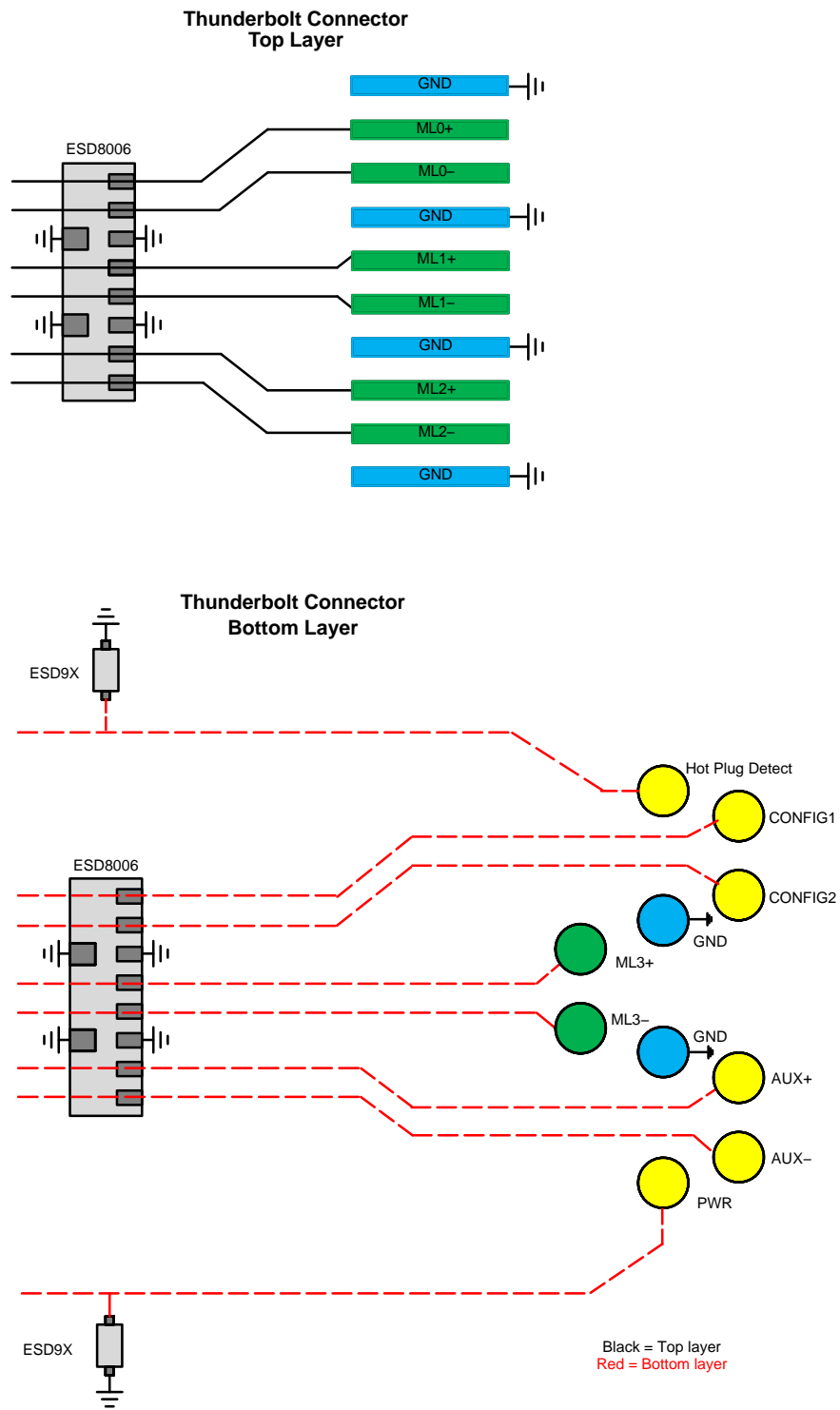


Figure 17. Thunderbolt Layout Diagram

PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
 - ♦ In USB 3.0 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in Figure 18. In this configuration, no DC current can flow through the ESD protection device preventing any potential

latch-up condition. For more information on latchup considerations, see below description on Page 11.

- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
 - ♦ Use curved traces when possible to avoid unwanted reflections.
 - ♦ Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
 - ♦ Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

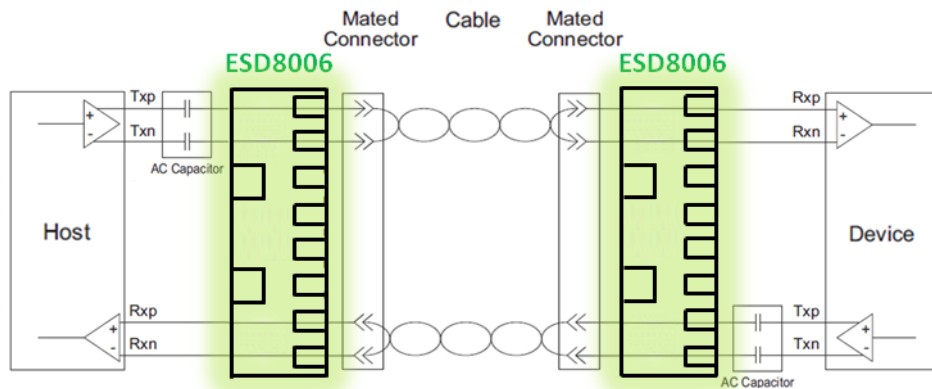


Figure 18. USB 3.0 Connection Diagram

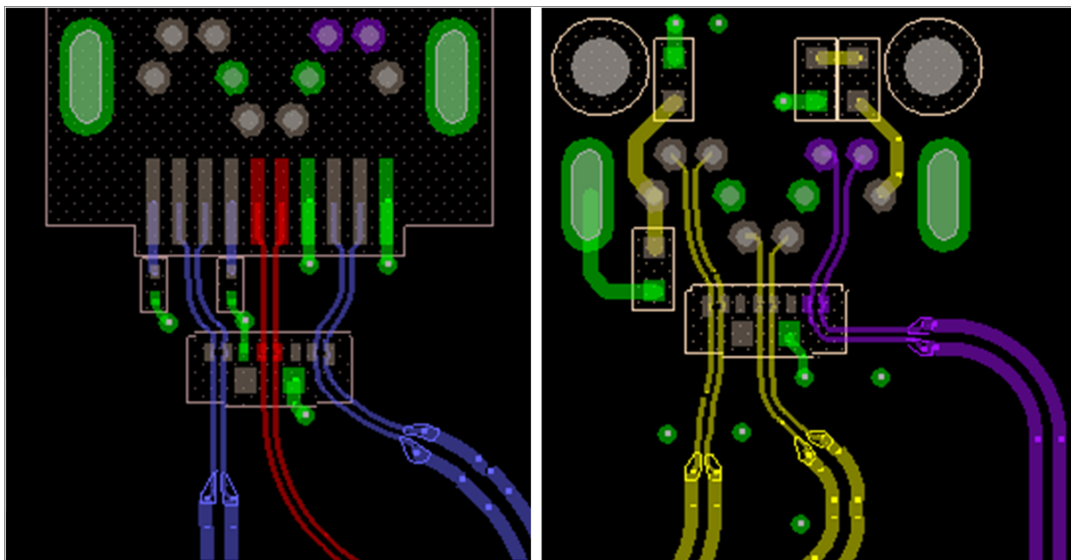


Figure 19. Thunderbolt Recommended PCB Layout

Latch-Up Considerations

ON Semiconductor's 8000 series of ESD protection devices utilize a snap-back, SCR type structure. By using this technology, the potential for a latch-up condition was taken into account by performing load line analysis of common high speed serial interfaces. Example load lines for latch-up free applications and applications with the potential for latch-up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch-up free load line case, the IV characteristic of the snapback protection device intersects the load-line in one unique point (V_{OP} , I_{OP}). This is the only stable operating point of the circuit and the system is

therefore latch-up free. Please note that for USB 3.0 applications, ESD8006 latch-up free considerations are explained in more detail in the above PCB layout guidelines. In the non-latch up free load line case, the IV characteristic of the snapback protection device intersects the load-line in two points (V_{OPA} , I_{OPA}) and (V_{OPB} , I_{OPB}). Therefore in this case, the potential for latch-up exists if the system settles at (V_{OPB} , I_{OPB}) after a transient. Because of this, ESD8006 should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch-up. Please refer to Application Note AND9116/D for a more in-depth explanation of latch-up considerations using ESD8000 series devices.

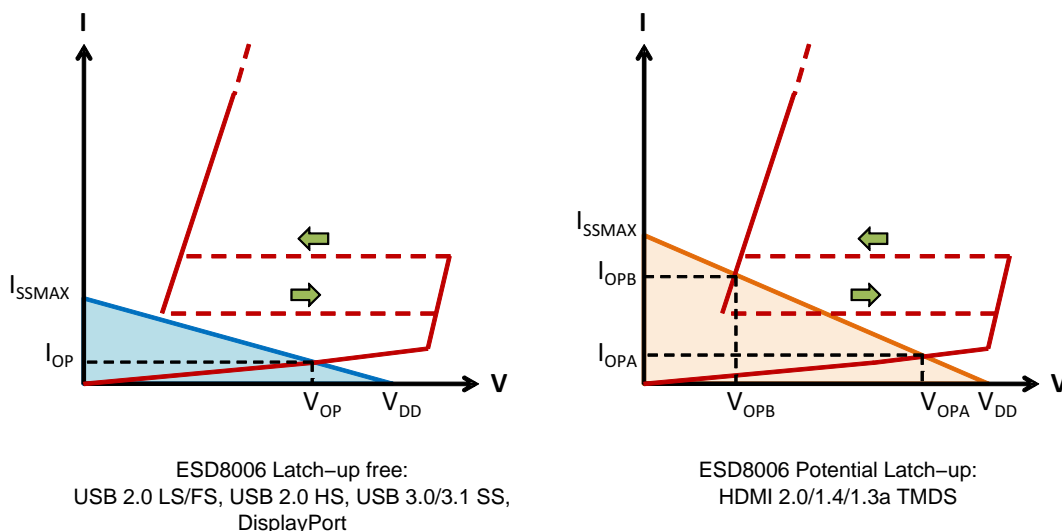


Figure 20. Example Load Lines for Latch-up Free Applications and Applications with the Potential for Latch-up

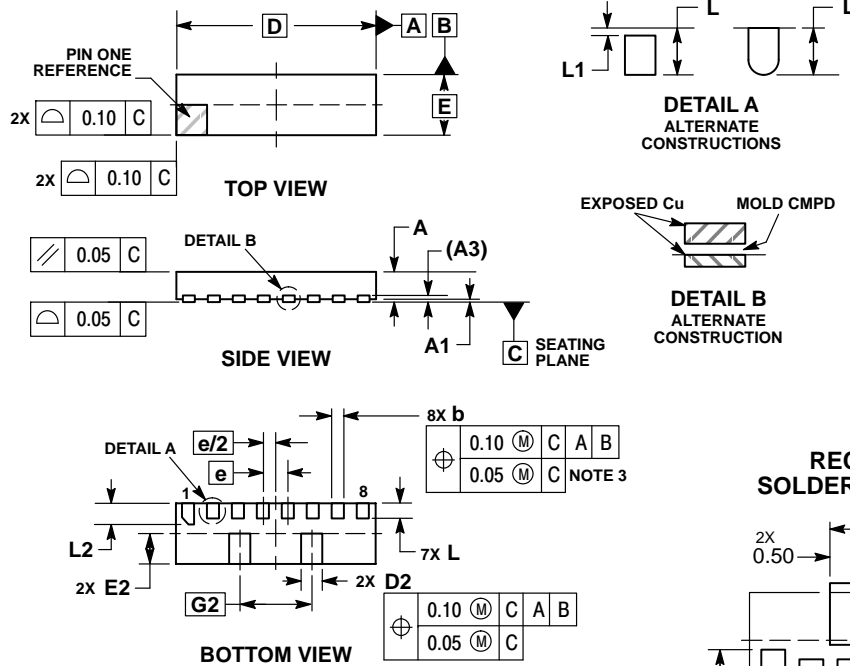
Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH-UP FREE APPLICATIONS

Application	VBR (min) (V)	IH (min) (mA)	VH (min) (V)	ON Semiconductor ESD8000 Series Recommended PN
HDMI 2.0/1.4/1.3a TMDS	3.465	54.78	1.0	ESD8104, ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004
USB 2.0 HS	0.482	N/A	1.0	ESD8004
USB 3.0/3.1 SS	2.800	N/A	1.0	ESD8004, ESD8006
DisplayPort	3.600	25.00	1.0	ESD8004, ESD8006

ESD8006

PACKAGE DIMENSIONS

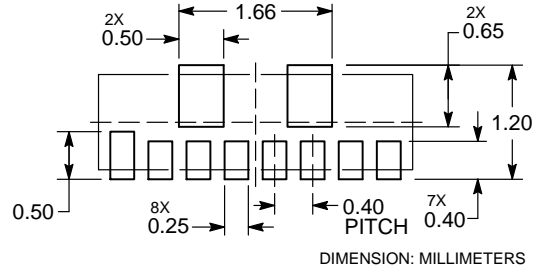
UDFN8, 3.3x1.0, 0.4P
CASE 517CB
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	3.30	BSC
D2	0.25	0.45
E	1.00	BSC
E2	0.45	0.55
e	0.40	BSC
G2	1.19	BSC
L	0.20	0.30
L1	—	0.15
L2	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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