NUP1301ML3T1G, SZNUP1301ML3T1G

Low Capacitance Diode Array for ESD Protection in a Single Data Line

NUP1301ML3T1G is a MicroIntegration device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (0.9 pF Maximum)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
  - Machine Model = Class C
  - Human Body Model = Class 3B
- Protection for IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- Pb−Free Package is Available*

Applications

- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I^2C Bus Protection

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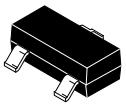
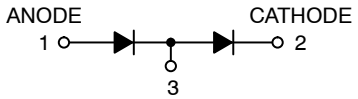
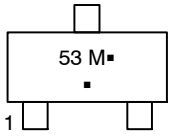


SOT−23
CASE 318
STYLE 11



MARKING DIAGRAM



53 = Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP1301ML3T1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
SZNUP1301ML3T1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS (Each Diode) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	70	Vdc
Forward Current	I_F	215	mAdc
Peak Forward Surge Current	$I_{FM(surge)}$	500	mAdc
Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	$I_{F(AV)}$	 715	mA
Repetitive Peak Forward Current	I_{FRM}	450	mA
Non−Repetitive Peak Forward Current t = 1.0 μs t = 1.0 ms t = 1.0 S	I_{FSM}	 2.0 1.0 0.5	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	625	°C/W
Lead Solder Temperature Maximum 10 Seconds Duration	T_L	 260	°C
Junction Temperature	T_J	−65 to 150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Reverse Breakdown Voltage ($I_{(BR)}$ = 100 μA)	$V_{(BR)}$	 70	 –	 –	Vdc
Reverse Voltage Leakage Current (V_R = 70 Vdc) (V_R = 25 Vdc, T_J = 150°C) (V_R = 70 Vdc, T_J = 150°C)	I_R	 – – –	 – – –	 2.5 30 50	μAdc
Diode Capacitance (between I/O and ground) (V_R = 0, f = 1.0 MHz)	C_D	 –	 –	 0.9	pF
Forward Voltage (I_F = 1.0 mAdc) (I_F = 10 mAdc) (I_F = 50 mAdc) (I_F = 150 mAdc)	V_F	 – – – –	 – – – –	 715 855 1000 1250	mV_{dc}

2. FR−5 = 1.0 × 0.75 × 0.062 in.
3. Alumina = 0.4 × 0.3 × 0.024 in, 99.5% alumina.
4. Include SZ-prefix devices where applicable.

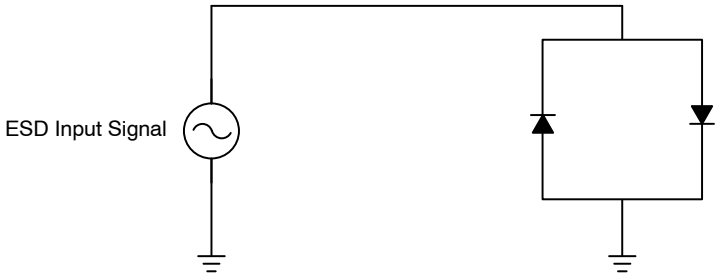


Figure 1. ESD Test Circuit

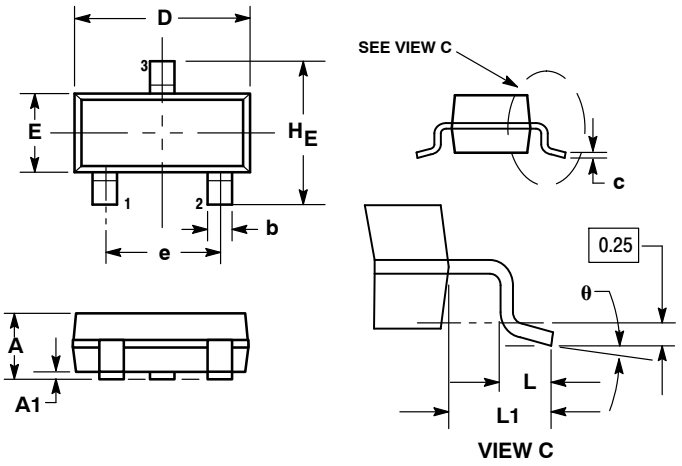
APPLICATION NOTE

Electrostatic Discharge

A common means of protecting high−speed data lines is to employ low−capacitance diode arrays in a rail−to−rail configuration. Two devices per line are connected between two fixed voltage references such as V_{CC} and ground. When the transient voltage exceeds the forward voltage (V_F) drop of the diode plus the reference voltage, the diodes direct the surge to the supply rail or ground. This method has several advantages including low loading capacitance, fast response time, and inherent bidirectionality (within the reference voltages). See Figure 1 for the test circuit used to verify the ESD rating for this device.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

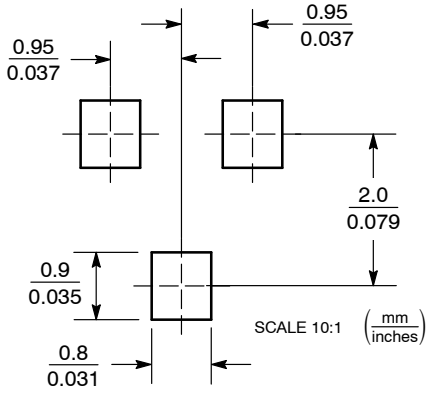


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

SOLDERING FOOTPRINT



PUBLICATION ORDERING INFORMATION

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