

# LMC6462 Dual/LMC6464 Quad Micropower, Rail-to-Rail Input and Output CMOS Operational Amplifier

Check for Samples: [LMC6462](#), [LMC6464](#)

## FEATURES

- (Typical Unless Otherwise Noted)
- Ultra Low Supply Current 20  $\mu$ A/Amplifier
- Ensured Characteristics at 3V and 5V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing
  - (within 10 mV of rail,  $V_S = 5V$  and  $R_L = 25$  k $\Omega$ )
- Low Input Current 150 fA
- Low Input Offset Voltage 0.25 mV

## APPLICATIONS

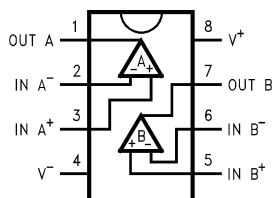
- Battery Operated Circuits
- Transducer Interface Circuits
- Portable Communication Devices
- Medical Applications
- Battery Monitoring

## DESCRIPTION

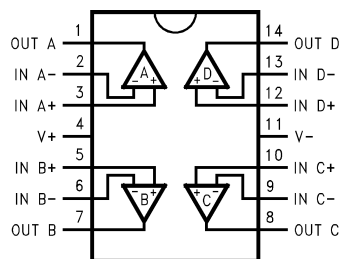
The LMC6462/4 is a micropower version of the popular LMC6482/4, combining Rail-to-Rail Input and Output Range with very low power consumption.

The LMC6462/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier, ensured for loads down to 25 k $\Omega$ , assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high voltage gain makes it unique among rail-to-rail amplifiers. The LMC6462/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

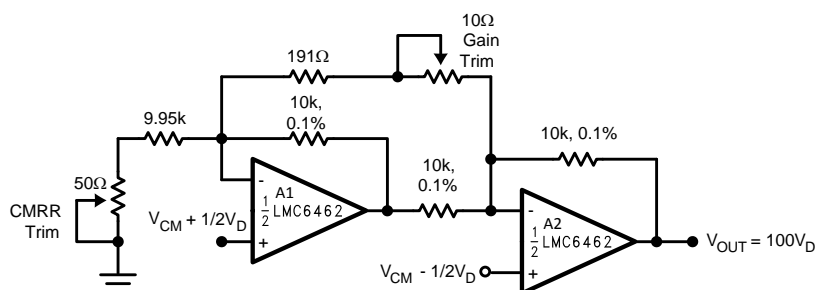
The LMC6462/4, with ensured specifications at 3V and 5V, is especially well-suited for low voltage applications. A quiescent power consumption of 60  $\mu$ W per amplifier (at  $V_S = 3V$ ) can extend the useful life of battery operated systems. The amplifier's 150 fA input current, low offset voltage of 0.25 mV, and 85 dB CMRR maintain accuracy in battery-powered systems.



**Figure 1. 8-Pin PDIP/SOIC – Top View**  
(See Package Number P or D)



**Figure 2. 14-Pin PDIP/SOIC – Top View**  
(See Package Number NFF0014A or D)



**Figure 3. Low-Power Two-Op-Amp Instrumentation Amplifier**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

|   |  |
|---|--|
| ESD Tolerance <sup>(4)</sup>                      | 2.0 kV   |
| Differential Input Voltage                        | ±Supply Voltage                                    |
| Voltage at Input/Output Pin                       | (V <sup>+</sup> ) + 0.3V, (V <sup>-</sup> ) - 0.3V |
| Supply Voltage (V <sup>+</sup> - V <sup>-</sup> ) | 16V  |
| Current at Input Pin <sup>(5)</sup>               | ±5 mA  |
| Current at Output Pin <sup>(6)(7)</sup>           | ±30 mA   |
| Current at Power Supply Pin                       | 40 mA  |
| Lead Temp. (Soldering, 10 sec.)                   | 260°C  |
| Storage Temperature Range                         | -65°C to +150°C                                    |
| Junction Temperature <sup>(8)</sup>               | 150°C  |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) For specified Military Temperature Range parameters see RETSMC6462/4X.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.
- (5) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- (6) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (7) Do not short circuit output to V<sup>+</sup>, when V<sup>+</sup> is greater than 13V or reliability will be adversely affected.
- (8) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly into a PC board.

### Operating Ratings

|                                       |                          |                                 |
|---------------------------------------|--------------------------|---------------------------------|
| Supply Voltage                        |                          | 3.0V ≤ V <sup>+</sup> ≤ 15.5V   |
| Junction Temperature Range            | LMC6462AM, LMC6464AM     | -55°C ≤ T <sub>J</sub> ≤ +125°C |
|                                       | LMC6462AI, LMC6464AI     | -40°C ≤ T <sub>J</sub> ≤ +85°C  |
|                                       | LMC6462BI, LMC6464BI     | -40°C ≤ T <sub>J</sub> ≤ +85°C  |
| Thermal Resistance (θ <sub>JA</sub> ) | P Package, 8-Pin PDIP    | 115°C/W                         |
|                                       | D Package, 8-Pin SOIC    | 193°C/W                         |
|                                       | NFF Package, 14-Pin PDIP | 81°C/W                          |
|                                       | D Package, 14-Pin SOIC   | 126°C/W                         |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

### 5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T<sub>J</sub> = 25°C, V<sup>+</sup> = 5V, V<sup>-</sup> = 0V, V<sub>CM</sub> = V<sub>O</sub> = V<sup>+</sup>/2 and R<sub>L</sub> > 1M. **Boldface** limits apply at the temperature extremes.

| Symbol            | Parameter                             | Conditions         | Typ <sup>(1)</sup> | LMC6462AI<br>LMC6464AI<br>Limit <sup>(2)</sup> | LMC6462BI<br>LMC6464BI<br>Limit <sup>(2)</sup> | LMC6462AM<br>LMC6464AM<br>Limit <sup>(2)</sup> | Units     |
|-------------------|---------------------------------------|--------------------|--------------------|--|--|--|-----------|
| V <sub>OS</sub>   | Input Offset Voltage                  |                    | 0.25               | 0.5<br><b>1.2</b>                              | 3.0<br><b>3.7</b>                              | 0.5<br><b>1.5</b>                              | mV<br>max |
| TCV <sub>OS</sub> | Input Offset Voltage<br>Average Drift |                    | 1.5                |  |  |  | μV/°C     |
| I <sub>B</sub>    | Input Current                         | See <sup>(3)</sup> | 0.15               | <b>10</b>                                      | <b>10</b>                                      | <b>200</b>                                     | pA max    |

- (1) Typical Values represent the most likely parametric norm.
- (2) All limits are specified by testing or statistical analysis.
- (3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

## 5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

| Symbol          | Parameter                                | Conditions  |          | Typ <sup>(1)</sup> | LMC6462AI<br>LMC6464AI<br>Limit <sup>(2)</sup> | LMC6462BI<br>LMC6464BI<br>Limit <sup>(2)</sup> | LMC6462AM<br>LMC6464AM<br>Limit <sup>(2)</sup> | Units       |
|-----------------|--|---|----------|--------------------|--|--|--|-------------|
| I <sub>OS</sub> | Input Offset Current                     | See <sup>(3)</sup>  |          | 0.075              | 5  | 5  | 100  | pA max      |
| C <sub>IN</sub> | Common-Mode<br>Input Capacitance         |   |          | 3                  |  |  |  | pF          |
| R <sub>IN</sub> | Input Resistance                         |   |          | >10                |  |  |  | Tera Ω      |
| CMRR            | Common Mode<br>Rejection Ratio           | 0V ≤ V <sub>CM</sub> ≤ 15.0V,<br>V <sup>+</sup> = 15V                       |          | 85                 | 70<br>67                                       | 65<br>62                                       | 70<br>65                                       | dB<br>min   |
|                 |  | 0V ≤ V <sub>CM</sub> ≤ 5.0V<br>V <sup>+</sup> = 5V                          |          | 85                 | 70<br>67                                       | 65<br>62                                       | 70<br>65                                       |             |
| +PSRR           | Positive Power Supply<br>Rejection Ratio | 5V ≤ V <sup>+</sup> ≤ 15V,<br>V <sup>-</sup> = 0V, V <sub>O</sub> = 2.5V    |          | 85                 | 70<br>67                                       | 65<br>62                                       | 70<br>65                                       | dB<br>min   |
| -PSRR           | Negative Power Supply<br>Rejection Ratio | -5V ≤ V <sup>-</sup> ≤ -15V,<br>V <sup>+</sup> = 0V, V <sub>O</sub> = -2.5V |          | 85                 | 70<br>67                                       | 65<br>62                                       | 70<br>65                                       | dB<br>min   |
| V <sub>CM</sub> | Input Common-Mode<br>Voltage Range       | V <sup>+</sup> = 5V<br>For CMRR ≥ 50 dB                                     |          | -0.2               | -0.10<br>0.00                                  | -0.10<br>0.00                                  | -0.10<br>0.00                                  | V<br>max    |
|                 |  |   |          | 5.30               | 5.25<br>5.00                                   | 5.25<br>5.00                                   | 5.25<br>5.00                                   | V<br>min    |
|                 |  | V <sup>+</sup> = 15V<br>For CMRR ≥ 50 dB                                    |          | -0.2               | -0.15<br>0.00                                  | -0.15<br>0.00                                  | -0.15<br>0.00                                  | V<br>max    |
|                 |  |   |          | 15.30              | 15.25<br>15.00                                 | 15.25<br>15.00                                 | 15.25<br>15.00                                 | V<br>min    |
| A <sub>V</sub>  | Large Signal<br>Voltage Gain             | R <sub>L</sub> = 100 kΩ <sup>(4)</sup>                                      | Sourcing | 3000               |  |  |  | V/mV<br>min |
|                 |  |   | Sinking  | 400                |  |  |  | V/mV<br>min |
|                 |  | R <sub>L</sub> = 25 kΩ <sup>(4)</sup>                                       | Sourcing | 2500               |  |  |  | V/mV<br>min |
|                 |  |   | Sinking  | 200                |  |  |  | V/mV<br>min |
| V <sub>O</sub>  | Output Swing                             | V <sup>+</sup> = 5V<br>R <sub>L</sub> = 100 kΩ to V <sup>+</sup> /2         |          | 4.995              | 4.990<br>4.980                                 | 4.950<br>4.925                                 | 4.990<br>4.970                                 | V<br>min    |
|                 |  |   |          | 0.005              | 0.010<br>0.020                                 | 0.050<br>0.075                                 | 0.010<br>0.030                                 | V<br>max    |
|                 |  | V <sup>+</sup> = 5V<br>R <sub>L</sub> = 25 kΩ to V <sup>+</sup> /2          |          | 4.990              | 4.975<br>4.965                                 | 4.950<br>4.850                                 | 4.975<br>4.955                                 | V<br>min    |
|                 |  |   |          | 0.010              | 0.020<br>0.035                                 | 0.050<br>0.150                                 | 0.020<br>0.045                                 | V<br>max    |
|                 |  | V <sup>+</sup> = 15V<br>R <sub>L</sub> = 100 kΩ to V <sup>+</sup> /2        |          | 14.990             | 14.975<br>14.965                               | 14.950<br>14.925                               | 14.975<br>14.955                               | V<br>min    |
|                 |  |   |          | 0.010              | 0.025<br>0.035                                 | 0.050<br>0.075                                 | 0.025<br>0.050                                 | V<br>max    |
|                 |  | V <sup>+</sup> = 15V<br>R <sub>L</sub> = 25 kΩ to V <sup>+</sup> /2         |          | 14.965             | 14.900<br>14.850                               | 14.850<br>14.800                               | 14.900<br>14.800                               | V<br>min    |
|                 |  |   |          | 0.025              | 0.050<br>0.150                                 | 0.100<br>0.200                                 | 0.050<br>0.200                                 | V<br>max    |

(4)  $V^+ = 15\text{V}$ ,  $V_{\text{CM}} = 7.5\text{V}$  and  $R_L$  connected to  $7.5\text{V}$ . For Sourcing tests,  $7.5\text{V} \leq V_O \leq 11.5\text{V}$ . For Sinking tests,  $3.5\text{V} \leq V_O \leq 7.5\text{V}$ .

## 5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

| Symbol          | Parameter  | Conditions   | Typ <sup>(1)</sup> | LMC6462AI<br>LMC6464AI<br>Limit <sup>(2)</sup> | LMC6462BI<br>LMC6464BI<br>Limit <sup>(2)</sup> | LMC6462AM<br>LMC6464AM<br>Limit <sup>(2)</sup> | Units                |
|-----------------|--|--|--------------------|--|--|--|----------------------|
| $I_{\text{SC}}$ | Output Short Circuit Current<br>$V^+ = 5\text{V}$  | Sourcing, $V_O = 0\text{V}$                          | 27                 | 19<br><b>15</b>                                | 19<br><b>15</b>                                | 19<br><b>15</b>                                | mA<br>min            |
|                 |  | Sinking, $V_O = 5\text{V}$                           | 27                 | 22<br><b>17</b>                                | 22<br><b>17</b>                                | 22<br><b>17</b>                                | mA<br>min            |
| $I_{\text{SC}}$ | Output Short Circuit Current<br>$V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$                          | 38                 | 24<br><b>17</b>                                | 24<br><b>17</b>                                | 24<br><b>17</b>                                | mA<br>min            |
|                 |  | Sinking, $V_O = 12\text{V}^{(5)}$                    | 75                 | 55<br><b>45</b>                                | 55<br><b>45</b>                                | 55<br><b>45</b>                                | mA<br>min            |
| $I_{\text{S}}$  | Supply Current                                     | Dual, LMC6462<br>$V^+ = +5\text{V}$ , $V_O = V^+/2$  | 40                 | 55<br><b>70</b>                                | 55<br><b>70</b>                                | 55<br><b>75</b>                                | $\mu\text{A}$<br>max |
|                 |  | Quad, LMC6464<br>$V^+ = +5\text{V}$ , $V_O = V^+/2$  | 80                 | 110<br><b>140</b>                              | 110<br><b>140</b>                              | 110<br><b>150</b>                              | $\mu\text{A}$<br>max |
|                 |  | Dual, LMC6462<br>$V^+ = +15\text{V}$ , $V_O = V^+/2$ | 50                 | 60<br><b>70</b>                                | 60<br><b>70</b>                                | 60<br><b>75</b>                                | $\mu\text{A}$<br>max |
|                 |  | Quad, LMC6464<br>$V^+ = +15\text{V}$ , $V_O = V^+/2$ | 90                 | 120<br><b>140</b>                              | 120<br><b>140</b>                              | 120<br><b>150</b>                              | $\mu\text{A}$<br>max |

(5) Do not short circuit output to  $V^+$ , when  $V^+$  is greater than 13V or reliability will be adversely affected.

## 5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

| Symbol   | Parameter                    | Conditions  | Typ <sup>(1)</sup> | LMC6462AI<br>LMC6464AI<br>Limit <sup>(2)</sup> | LMC6462BI<br>LMC6464BI<br>Limit <sup>(2)</sup> | LMC6462AM<br>LMC6464AM<br>Limit <sup>(2)</sup> | Units                        |
|----------|------------------------------|---|--------------------|--|--|--|------------------------------|
| SR       | Slew Rate                    | See <sup>(3)</sup>                                | 28                 | 15<br><b>8</b>                                 | 15<br><b>8</b>                                 | 15<br><b>8</b>                                 | V/ms<br>min                  |
| GBW      | Gain-Bandwidth Product       | $V^+ = 15\text{V}$                                | 50                 |  |  |  | kHz                          |
| $\phi_m$ | Phase Margin                 |   | 50                 |  |  |  | Deg                          |
| $G_m$    | Gain Margin                  |   | 15                 |  |  |  | dB                           |
|          | Amp-to-Amp Isolation         | See <sup>(4)</sup>                                | 130                |  |  |  | dB                           |
| $e_n$    | Input-Referred Voltage Noise | $f = 1\text{ kHz}$<br>$V_{\text{CM}} = 1\text{V}$ | 80                 |  |  |  | $\text{nV}/\sqrt{\text{Hz}}$ |
| $i_n$    | Input-Referred Current Noise | $f = 1\text{ kHz}$                                | 0.03               |  |  |  | $\text{pA}/\sqrt{\text{Hz}}$ |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3)  $V^+ = 15\text{V}$ . Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

(4) Input referred,  $V^+ = 15\text{V}$  and  $R_L = 100\text{ k}\Omega$  connected to 7.5V. Each amp excited in turn with 1 kHz to produce  $V_O = 12\text{ V}_{\text{pp}}$ .

### 3V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

| Symbol     | Parameter                             | Conditions   | Typ <sup>(1)</sup> | LMC6462AI<br>LMC6464AI<br>Limit <sup>(2)</sup> | LMC6462BI<br>LMC6464BI<br>Limit <sup>(2)</sup> | LMC6462AM<br>LMC6464AM<br>Limit <sup>(2)</sup> | Units                        |
|------------|---------------------------------------|--|--------------------|--|--|--|------------------------------|
| $V_{OS}$   | Input Offset Voltage                  |  | 0.9                | 2.0<br><b>2.7</b>                              | 3.0<br><b>3.7</b>                              | 2.0<br><b>3.0</b>                              | mV<br>max                    |
| $TCV_{OS}$ | Input Offset Voltage<br>Average Drift |  | 2.0                |  |  |  | $\mu\text{V}/^\circ\text{C}$ |
| $I_B$      | Input Current                         | See <sup>(3)</sup>                                       | 0.15               | <b>10</b>                                      | <b>10</b>                                      | <b>200</b>                                     | pA                           |
| $I_{OS}$   | Input Offset Current                  | See <sup>(3)</sup>                                       | 0.075              | <b>5</b>                                       | <b>5</b>                                       | <b>100</b>                                     | pA                           |
| CMRR       | Common Mode<br>Rejection Ratio        | $0\text{V} \leq V_{CM} \leq 3\text{V}$                   | 74                 | 60   | 60   | 60   | dB<br>min                    |
| PSRR       | Power Supply<br>Rejection Ratio       | $3\text{V} \leq V^+ \leq 15\text{V}$ , $V^- = 0\text{V}$ | 80                 | 60   | 60   | 60   | dB<br>min                    |
| $V_{CM}$   | Input Common-Mode<br>Voltage Range    | For CMRR $\geq 50$ dB                                    | -0.10              | 0.0  | 0.0  | 0.0  | V<br>max                     |
|            |                                       |  | 3.0                | 3.0  | 3.0  | 3.0  | V<br>min                     |
| $V_O$      | Output Swing                          | $R_L = 25\text{ k}\Omega$ to $V^+/2$                     | 2.95               | 2.9  | 2.9  | 2.9  | V<br>min                     |
|            |                                       |  | 0.15               | 0.1  | 0.1  | 0.1  | V<br>max                     |
| $I_S$      | Supply Current                        | Dual, LMC6462<br>$V_O = V^+/2$                           | 40                 | 55<br><b>70</b>                                | 55<br><b>70</b>                                | 55<br><b>70</b>                                | $\mu\text{A}$                |
|            |                                       | Quad, LMC6464<br>$V_O = V^+/2$                           | 80                 | 110<br><b>140</b>                              | 110<br><b>140</b>                              | 110<br><b>140</b>                              | $\mu\text{A}$<br>max         |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

### 3V AC Electrical Characteristics

Unless otherwise specified,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface limits** apply at the temperature extremes.

| Symbol | Parameter              | Conditions         | Typ <sup>(1)</sup> | LMC6462AI<br>LMC6464AI<br>Limit <sup>(2)</sup> | LMC6462BI<br>LMC6464BI<br>Limit <sup>(2)</sup> | LMC6462AM<br>LMC6464AM<br>Limit <sup>(2)</sup> | Units |
|--------|------------------------|--------------------|--------------------|--|--|--|-------|
| SR     | Slew Rate              | See <sup>(3)</sup> | 23                 |  |  |  | V/ms  |
| GBW    | Gain-Bandwidth Product |                    | 50                 |  |  |  | kHz   |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

## Typical Performance Characteristics

$V_S = +5V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

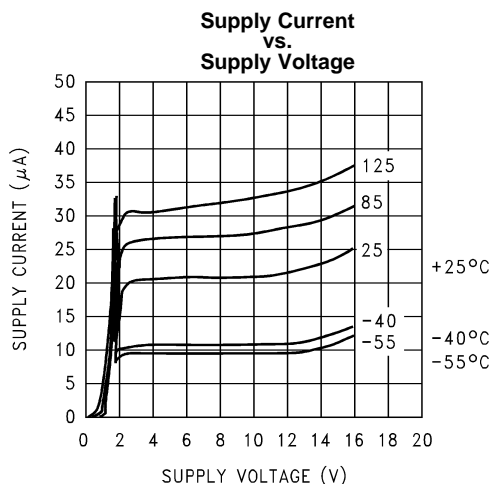


Figure 4.

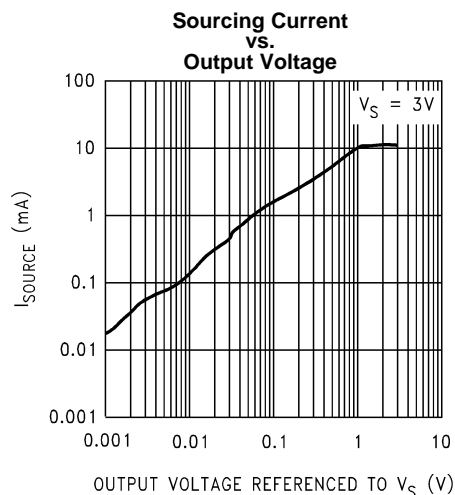


Figure 5.

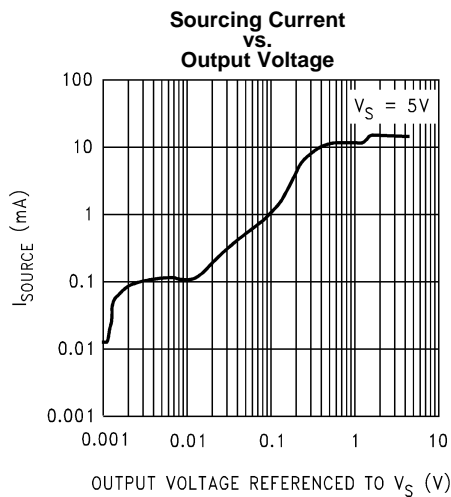


Figure 6.

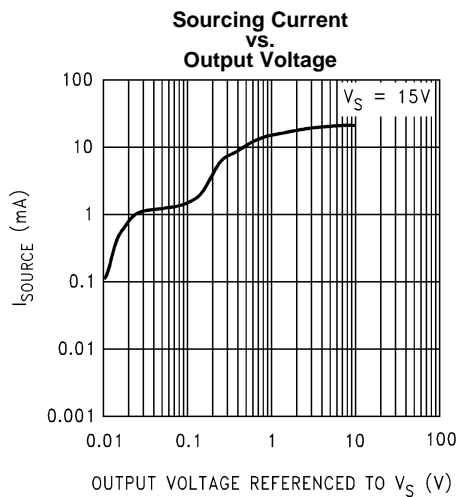


Figure 7.

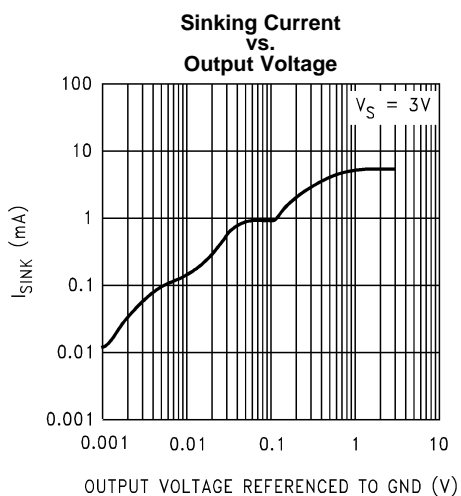


Figure 8.

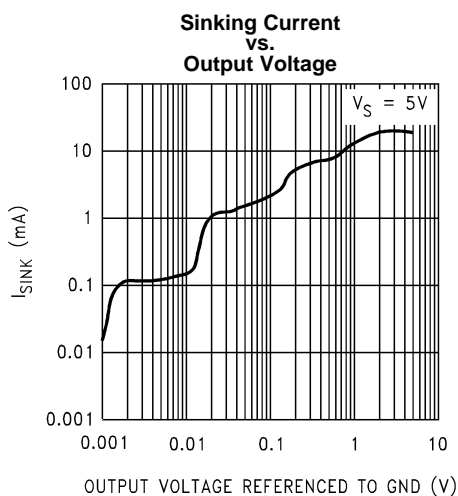
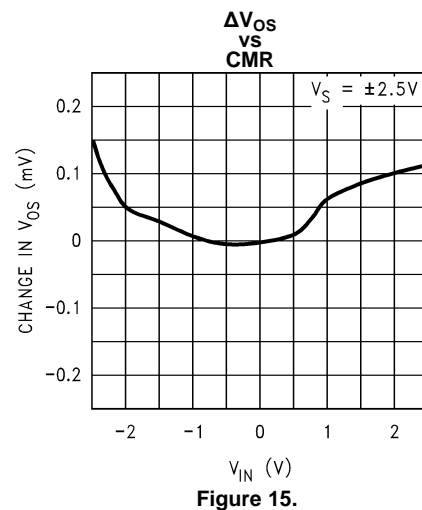
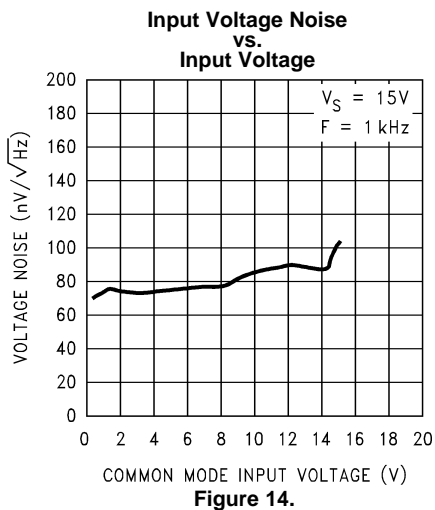
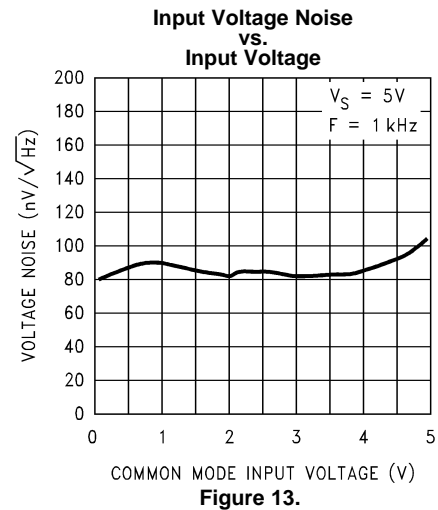
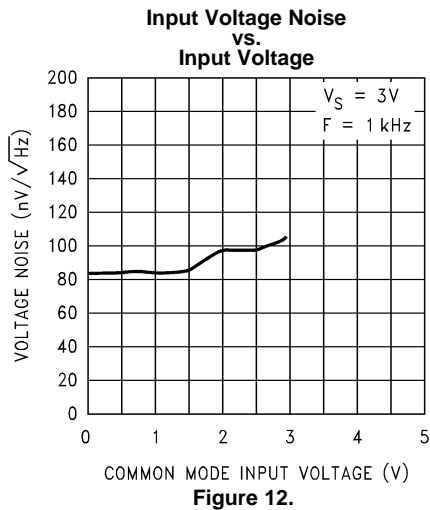
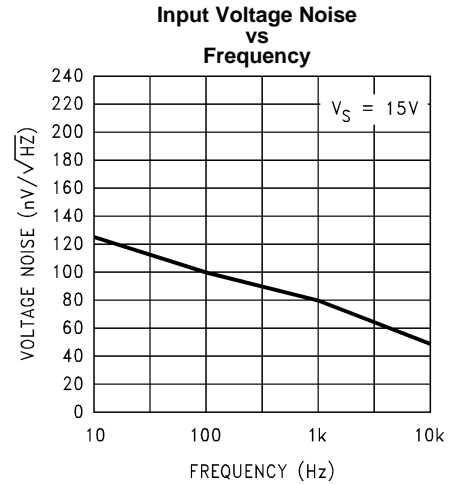
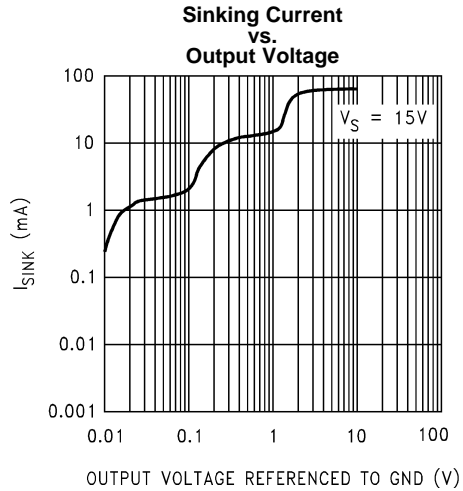


Figure 9.

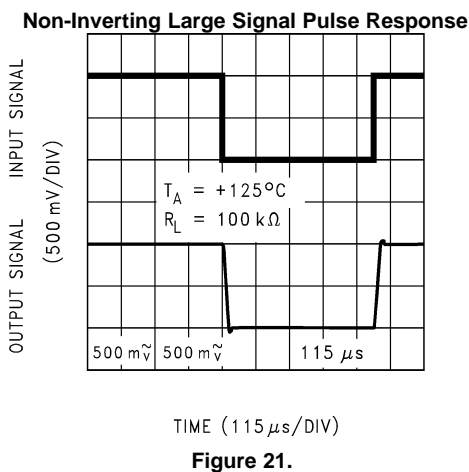
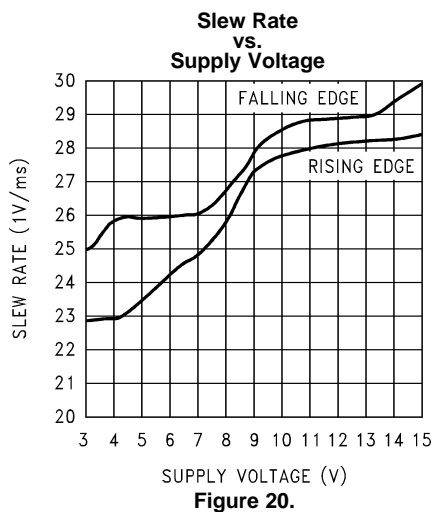
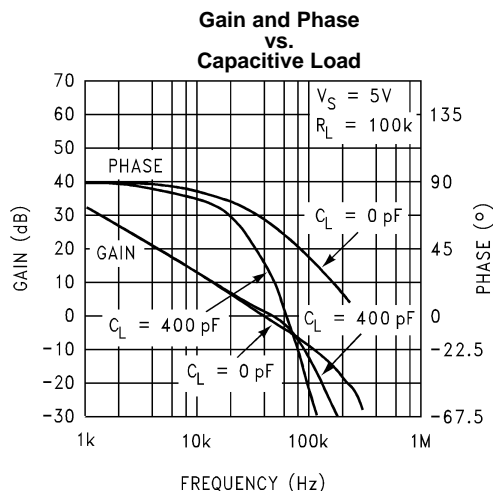
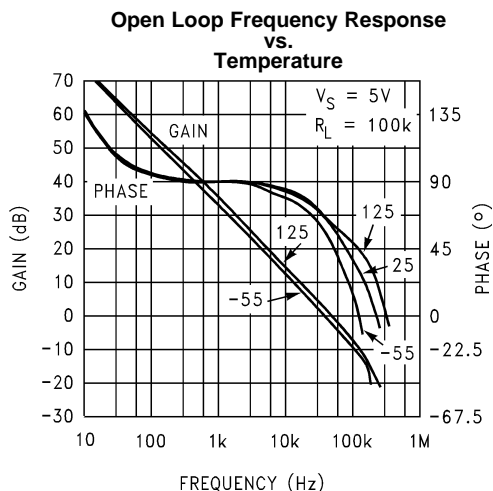
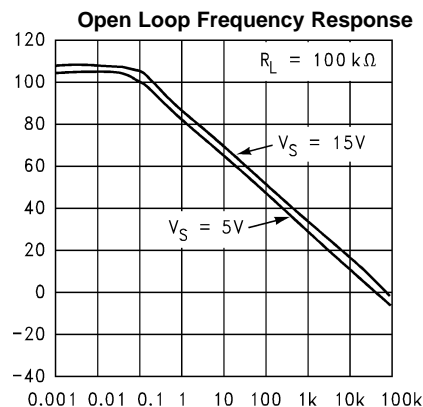
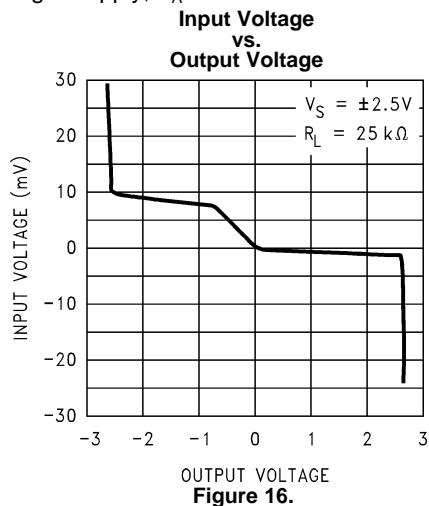
## Typical Performance Characteristics (continued)

$V_S = +5V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified



### Typical Performance Characteristics (continued)

$V_S = +5V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

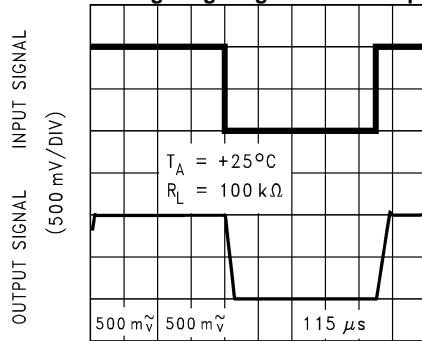




## Typical Performance Characteristics (continued)

$V_S = +5V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

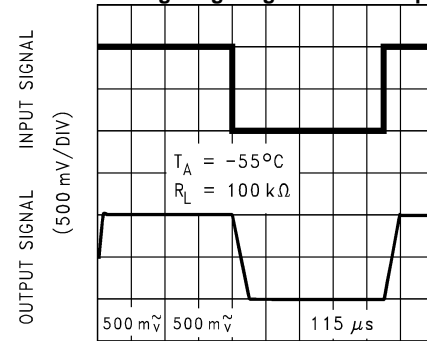
**Non-Inverting Large Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 22.**

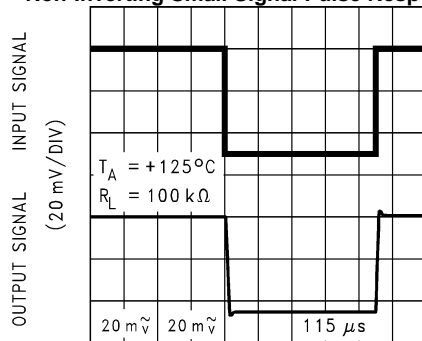
**Non-Inverting Large Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 23.**

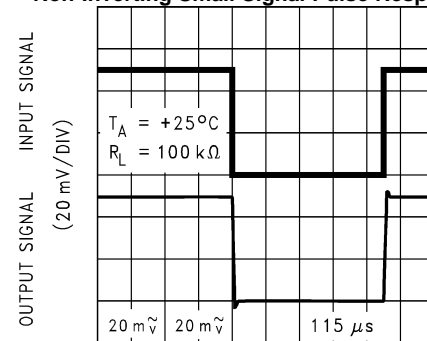
**Non-Inverting Small Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 24.**

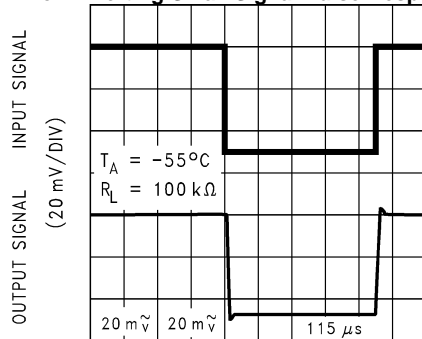
**Non-Inverting Small Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 25.**

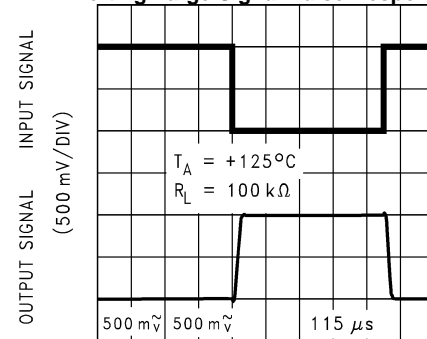
**Non-Inverting Small Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 26.**

**Inverting Large Signal Pulse Response**



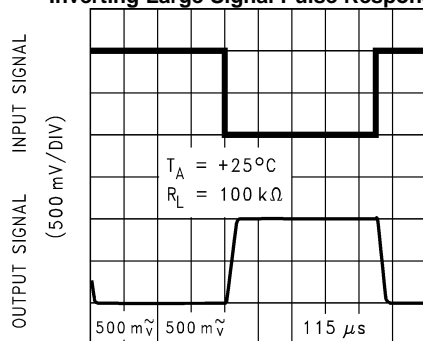
TIME (115  $\mu s$ /DIV)

**Figure 27.**

### Typical Performance Characteristics (continued)

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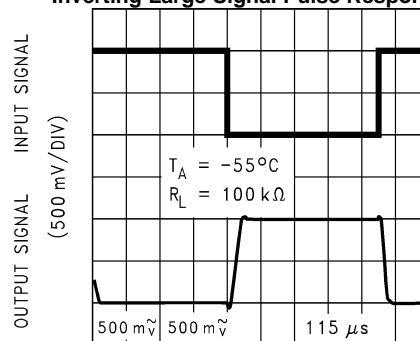
**Inverting Large Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 28.**

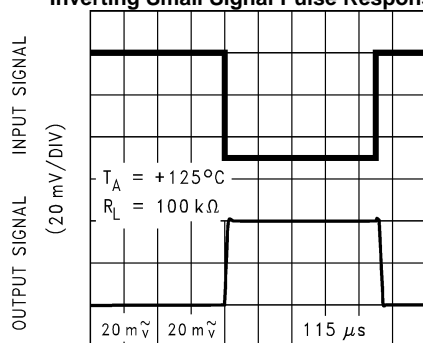
**Inverting Large Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 29.**

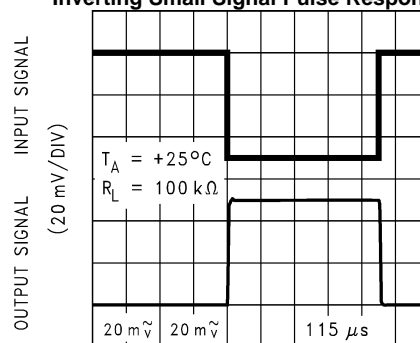
**Inverting Small Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 30.**

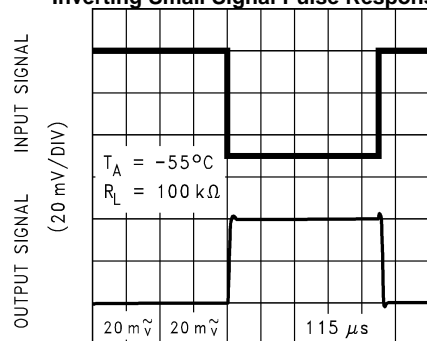
**Inverting Small Signal Pulse Response**



TIME (115  $\mu s$ /DIV)

**Figure 31.**

**Inverting Small Signal Pulse Response**



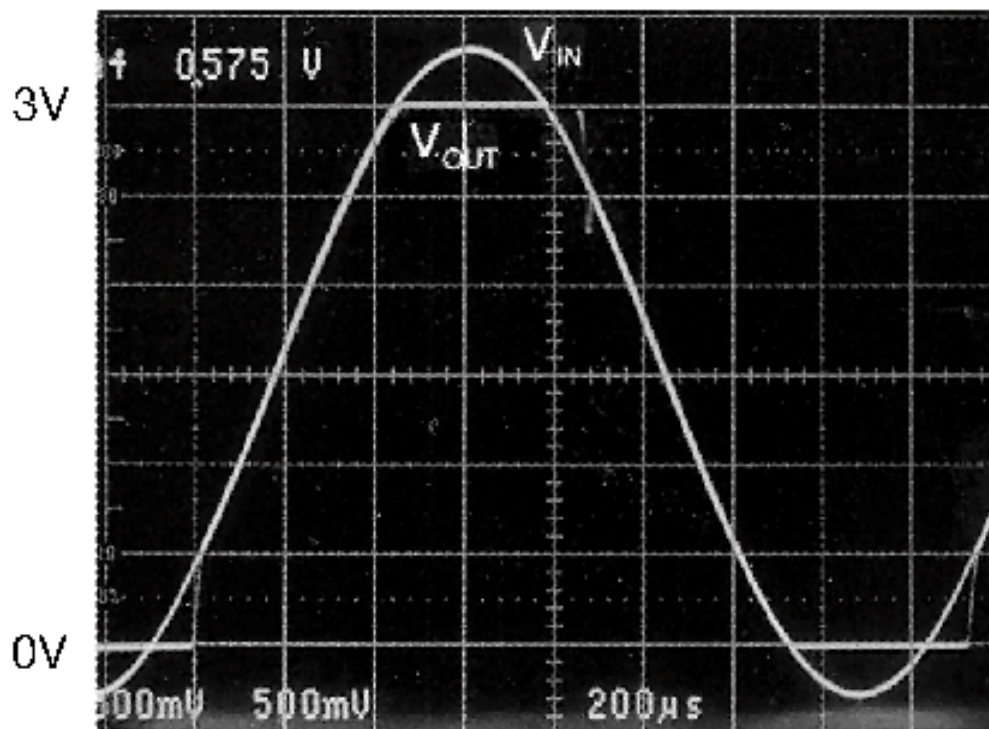
TIME (115  $\mu s$ /DIV)

**Figure 32.**

## APPLICATION INFORMATION

### Input Common-Mode Voltage Range

The LMC6462/4 has a rail-to-rail input common-mode voltage range. [Figure 33](#) shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



**Figure 33. An Input Voltage Signal Exceeds the LMC6462/4 Power Supply Voltage with No Output Phase Inversion**

The absolute maximum input voltage at  $V^+ = 3V$  is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in [Figure 34](#), can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to  $\pm 5$  mA, with an input resistor, as shown in [Figure 35](#).

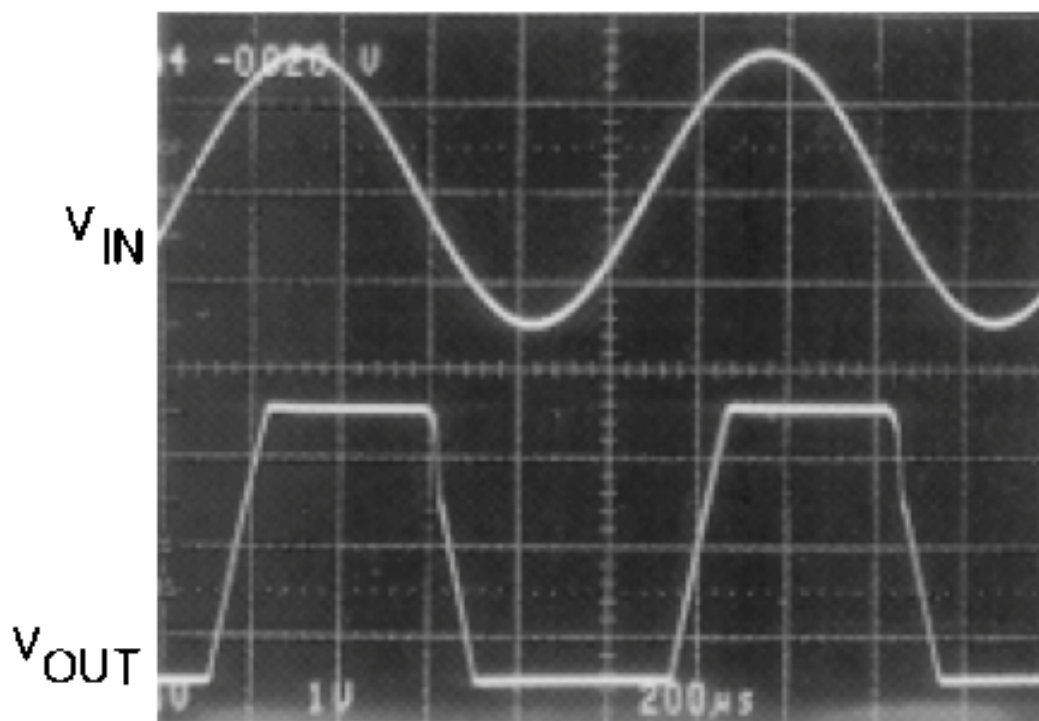


Figure 34. A  $\pm 7.5\text{V}$  Input Signal Greatly Exceeds the 3V Supply in Figure 35 Causing No Phase Inversion Due to  $R_I$

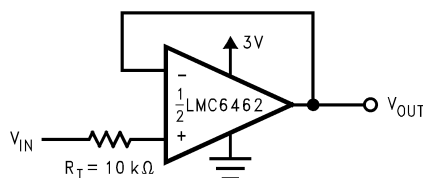


Figure 35. Input Current Protection for Voltages Exceeding the Supply Voltage

## Rail-to-Rail Output

The approximated output resistance of the LMC6462/4 is  $180\Omega$  sourcing, and  $130\Omega$  sinking at  $V_S = 3\text{V}$ , and  $110\Omega$  sourcing and  $83\Omega$  sinking at  $V_S = 5\text{V}$ . The maximum output swing can be estimated as a function of load using the calculated output resistance.

## Capacitive Load Tolerance

The LMC6462/4 can typically drive a  $200\text{ pF}$  load with  $V_S = 5\text{V}$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 36. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.

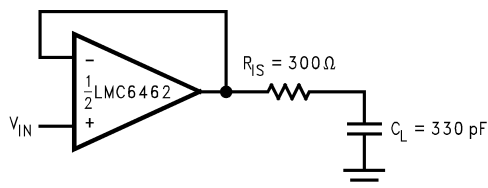


Figure 36. Resistive Isolation of a 300 pF Capacitive Load

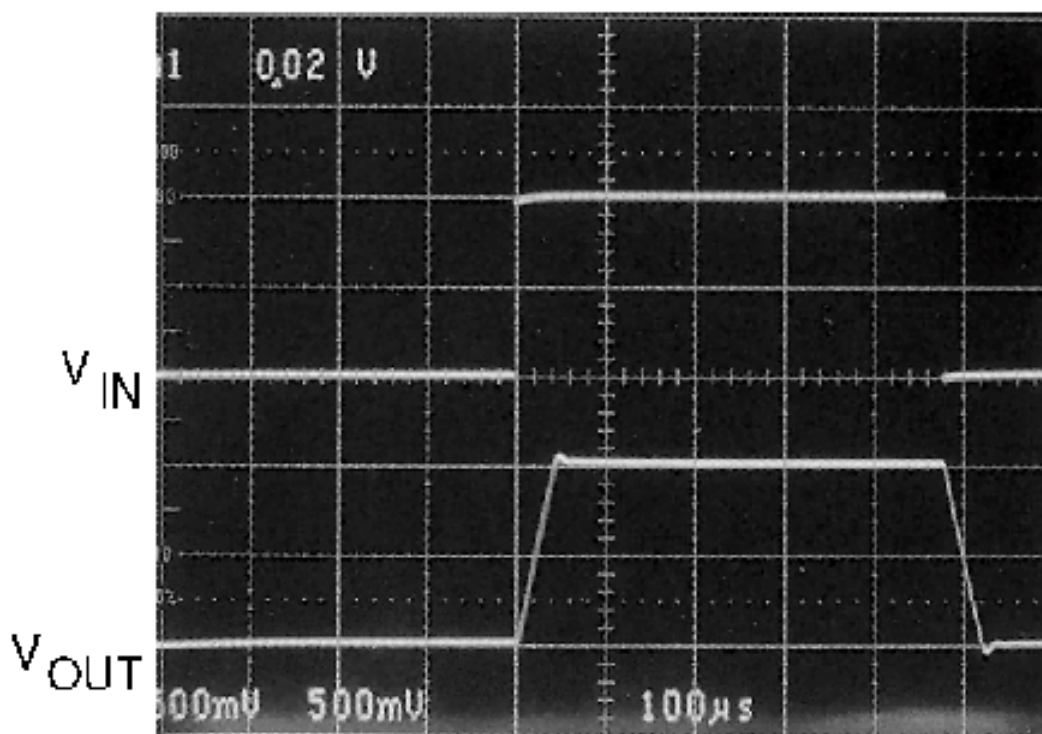
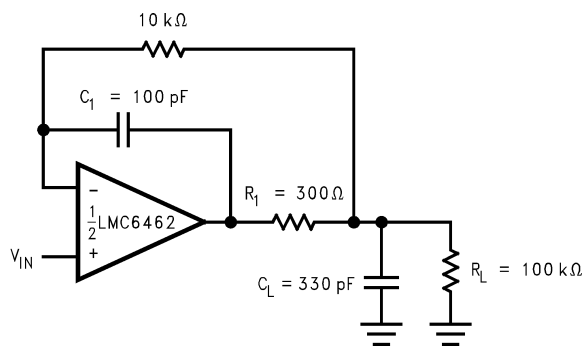


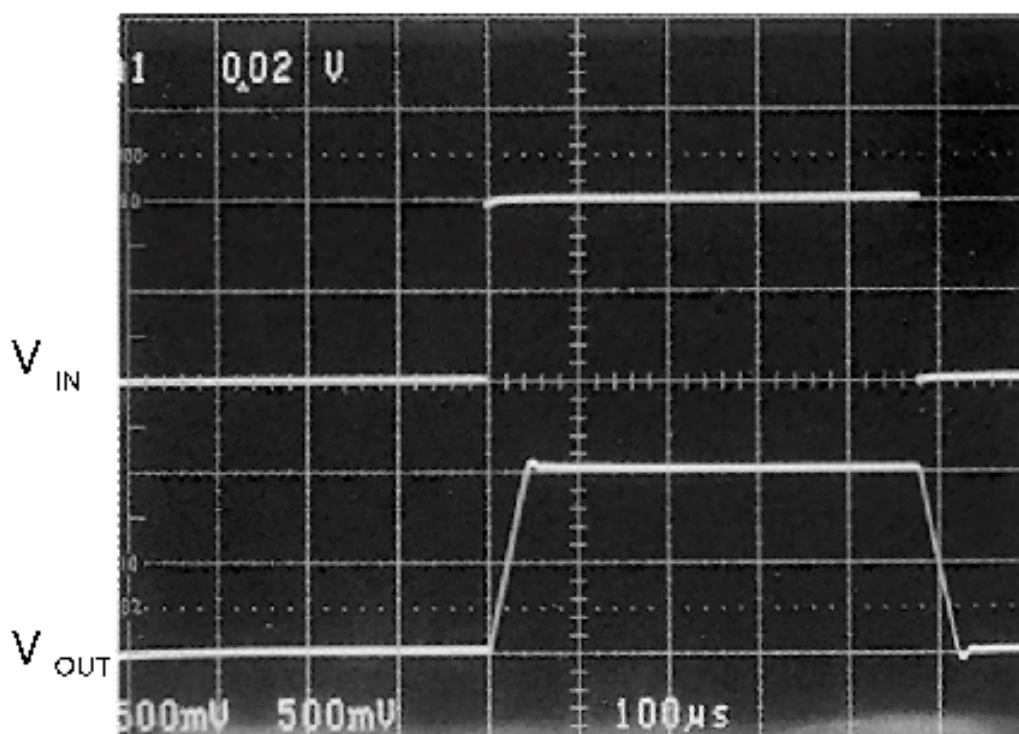
Figure 37. Pulse Response of the LMC6462 Circuit Shown in Figure 36

Figure 37 displays the pulse response of the LMC6462/4 circuit in Figure 36.

Another circuit, shown in Figure 38, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown in Figure 36 because it provides DC accuracy as well as AC stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.



**Figure 38. LMC6462 Non-Inverting Amplifier, Compensated to Handle a 300 pF Capacitive and 100 kΩ Resistive Load**



**Figure 39. Pulse Response of LMC6462 Circuit in Figure 38**

The pulse response of the circuit shown in Figure 38 is shown in Figure 39

### Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6462/4. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

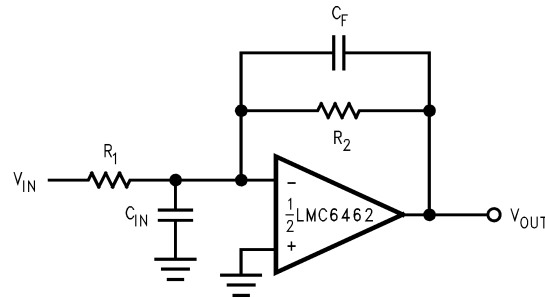


Figure 40. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 40),  $C_F$ , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_F \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for  $C_F$  may be different. The values of  $C_F$  should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

## Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 41 and Figure 42. Large value resistances and potentiometers are used to reduce power consumption while providing typically  $\pm 2.5$  mV of adjustment range, referred to the input, for both configurations with  $V_S = \pm 5$ V.

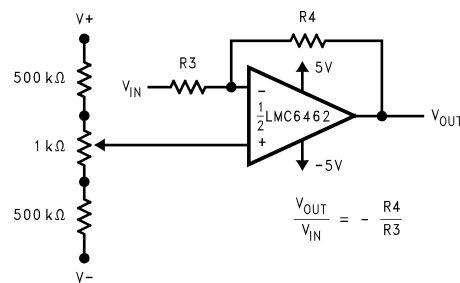


Figure 41. Inverting Configuration Offset Voltage Adjustment

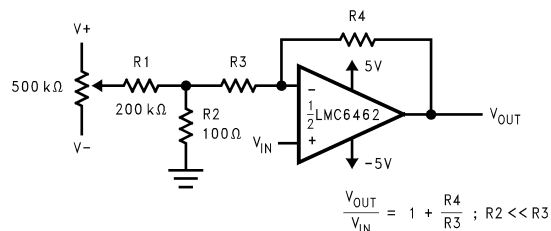


Figure 42. Non-Inverting Configuration Offset Voltage Adjustment

## SPICE Macromodel

A Spice macromodel is available for the LMC6462/4. This model includes a simulation of:

- Input common-mode voltage range



- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

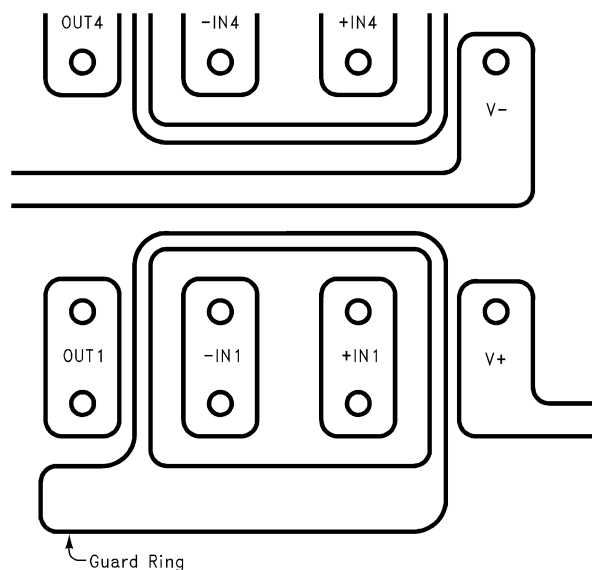
and many more characteristics as listed on the macromodel disk.

Contact the Texas Instruments Customer Response Center to obtain an operational amplifier Spice model library disk

### Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6462/4, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6462's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 43. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 30 times degradation from the LMC6462/4's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of  $10^{11}\Omega$  would cause only 0.05 pA of leakage current. See Figure 44 through Figure 46 for typical connections of guard rings for standard op-amp configurations.



**Figure 43. Example of Guard Ring in P.C. Board Layout**



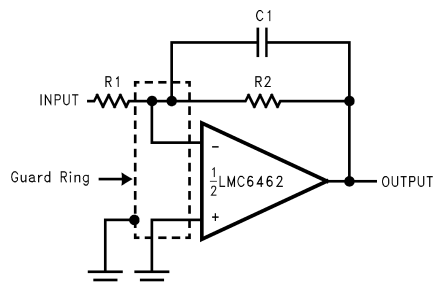


Figure 44. Typical Connections of Guard Rings – Inverting Amplifier

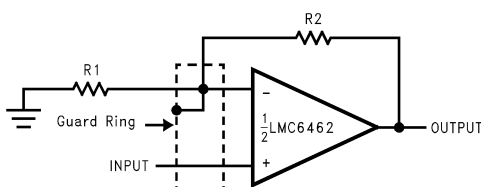


Figure 45. Typical Connections of Guard Rings – Non-Inverting Amplifier

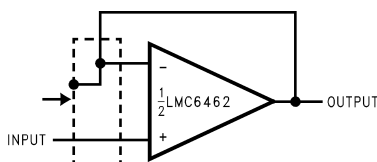
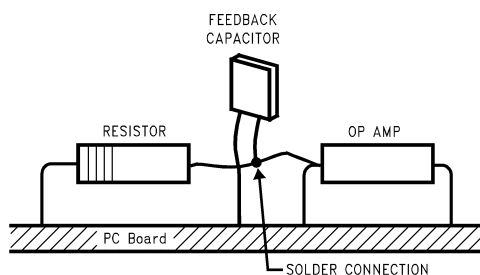


Figure 46. Typical Connections of Guard Rings – Follower

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 47.



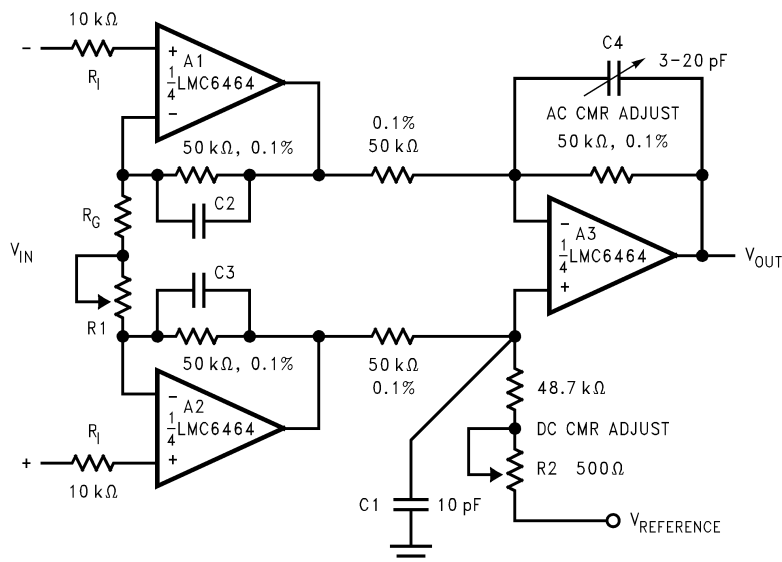
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 47. Air Wiring

## Instrumentation Circuits

The LMC6464 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6464 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6464 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

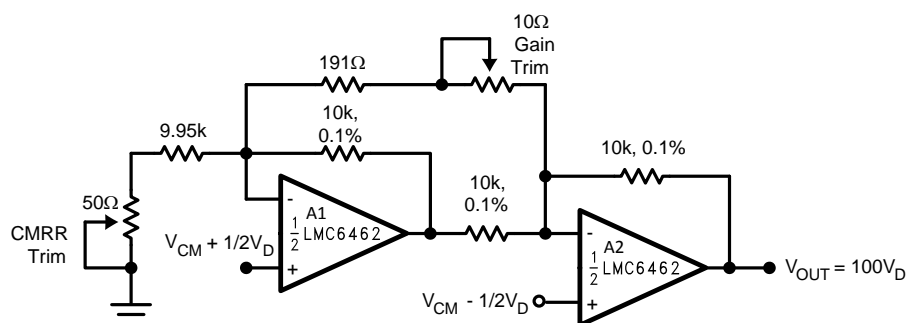
A small valued potentiometer is used in series with  $R_G$  to set the differential gain of the three op-amp instrumentation circuit in [Figure 48](#). This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.



### Figure 48. Low Power Three Op-Amp Instrumentation Amplifier

A two op-amp instrumentation amplifier designed for a gain of 100 is shown in [Figure 49](#). Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.



### Figure 49. Low-Power Two-Op-Amp Instrumentation Amplifier

## TYPICAL SINGLE-SUPPLY APPLICATIONS

### Transducer Interface Circuits

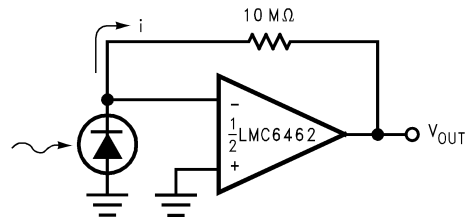


Figure 50. Photo Detector Circuit

Photocells can be used in portable light measuring instruments. The LMC6462, which can be operated off a battery, is an excellent choice for this circuit because of its very low input current and offset voltage.

### LMC6462 as a Comparator

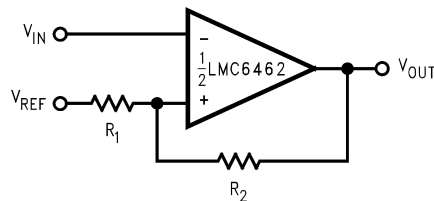


Figure 51. Comparator with Hysteresis

Figure 51 shows the application of the LMC6462 as a comparator. The hysteresis is determined by the ratio of the two resistors. The LMC6462 can thus be used as a micropower comparator, in applications where the quiescent current is an important parameter.

### Half-Wave and Full-Wave Rectifiers

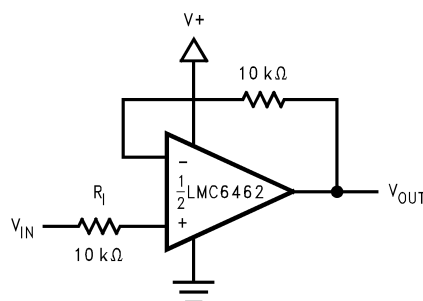


Figure 52. Half-Wave Rectifier with Input Current Protection ( $R_I$ )

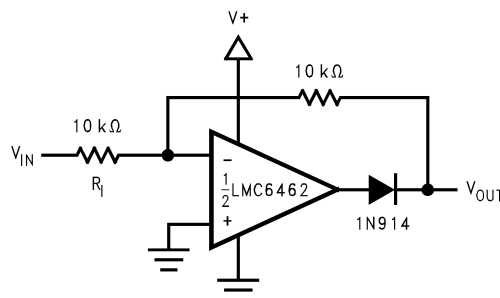
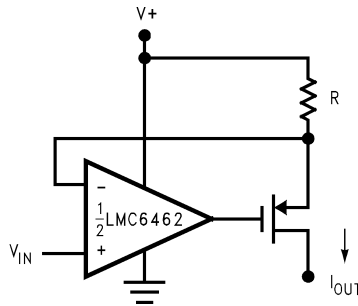


Figure 53. Full-Wave Rectifier with Input Current Protection ( $R_I$ )

In [Figure 52](#) [Figure 53](#),  $R_1$  limits current into the amplifier since excess current can be caused by the input voltage exceeding the supply voltage.

### Precision Current Source

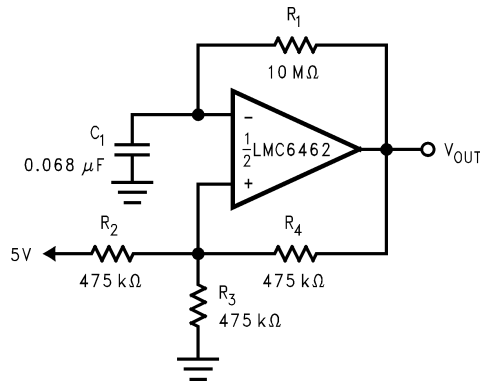


**Figure 54. Precision Current Source**

The output current  $I_{OUT}$  is given by:

$$I_{OUT} = \left( \frac{V^+ - V_{IN}}{R} \right) \quad (3)$$

### Oscillators



**Figure 55. 1 Hz Square-Wave Oscillator**

For single supply 5V operation, the output of the circuit will swing from 0V to 5V. The voltage divider set up  $R_2$ ,  $R_3$  and  $R_4$  will cause the non-inverting input of the LMC6462 to move from 1.67V ( $\frac{1}{3}$  of 5V) to 3.33V ( $\frac{2}{3}$  of 5V). This voltage behaves as the threshold voltage.

$R_1$  and  $C_1$  determine the time constant of the circuit. The frequency of oscillation,  $f_{OSC}$  is

$$\left( \frac{1}{2\Delta t} \right) \quad (4)$$

where  $\Delta t$  is the time the amplifier input takes to move from 1.67V to 3.33V. The calculations are shown below.

$$1.67 = 5 \left( 1 - e^{-\frac{t_1}{\tau}} \right) \quad (5)$$

where  $\tau = RC = 0.68$  seconds

$\rightarrow t_1 = 0.27$  seconds.

and

$$3.33 = 5 \left( 1 - e^{-\frac{t_2}{\tau}} \right) \quad (6)$$

$\rightarrow t_2 = 0.75$  seconds

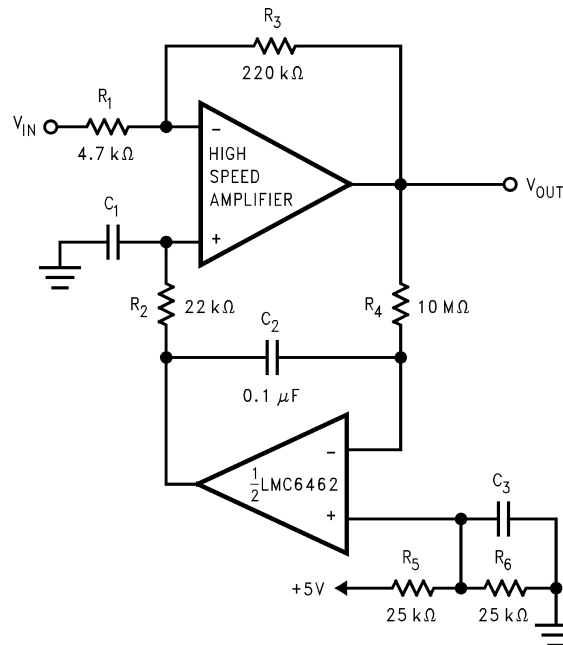
Then,

$$f_{\text{osc}} = \left( \frac{1}{2\Delta t} \right) \quad (7)$$

$$= \frac{1}{2(0.75 - 0.27)} \quad (8)$$

= 1 Hz

## Low Frequency Null



**Figure 56. High Gain Amplifier with Low Frequency Null**

Output offset voltage is the error introduced in the output voltage due to the inherent input offset voltage  $V_{\text{OS}}$ , of an amplifier.

Output Offset Voltage = (Input Offset Voltage) (Gain)

In the above configuration, the resistors  $R_5$  and  $R_6$  determine the nominal voltage around which the input signal,  $V_{\text{IN}}$  should be symmetrical. The high frequency component of the input signal  $V_{\text{IN}}$  will be unaffected while the low frequency component will be nulled since the DC level of the output will be the input offset voltage of the LMC6462 plus the bias voltage. This implies that the output offset voltage due to the top amplifier will be eliminated.

## REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D   | Page |
|--|------|
| <ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul> | 21   |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMC6462AIM       | NRND          | SOIC         | D                  | 8    | 95             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC64<br>62AIM          |                         |
| LMC6462AIM/NOPB  | ACTIVE        | SOIC         | D                  | 8    | 95             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC64<br>62AIM          | <a href="#">Samples</a> |
| LMC6462AIMX      | NRND          | SOIC         | D                  | 8    |                | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC64<br>62AIM          |                         |
| LMC6462AIMX/NOPB | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC64<br>62AIM          | <a href="#">Samples</a> |
| LMC6462AIN       | LIFEBUY       | PDIP         | P                  | 8    | 40             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6462<br>AIN          |                         |
| LMC6462AIN/NOPB  | ACTIVE        | PDIP         | P                  | 8    | 40             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-NA-UNLIM     | -40 to 85    | LMC6462<br>AIN          | <a href="#">Samples</a> |
| LMC6462BIM/NOPB  | ACTIVE        | SOIC         | D                  | 8    | 95             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC64<br>62BIM          | <a href="#">Samples</a> |
| LMC6462BIMX/NOPB | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC64<br>62BIM          | <a href="#">Samples</a> |
| LMC6462BIN       | LIFEBUY       | PDIP         | P                  | 8    | 40             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6462<br>BIN          |                         |
| LMC6462BIN/NOPB  | ACTIVE        | PDIP         | P                  | 8    | 40             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-NA-UNLIM     | -40 to 85    | LMC6462<br>BIN          | <a href="#">Samples</a> |
| LMC6464AIM       | NRND          | SOIC         | D                  | 14   | 55             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6464<br>AIM          |                         |
| LMC6464AIM/NOPB  | ACTIVE        | SOIC         | D                  | 14   | 55             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC6464<br>AIM          | <a href="#">Samples</a> |
| LMC6464AIMX      | NRND          | SOIC         | D                  | 14   | 2500           | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6464<br>AIM          |                         |
| LMC6464AIMX/NOPB | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC6464<br>AIM          | <a href="#">Samples</a> |
| LMC6464BIM       | NRND          | SOIC         | D                  | 14   | 55             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6464<br>BIM          |                         |
| LMC6464BIM/NOPB  | ACTIVE        | SOIC         | D                  | 14   | 55             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC6464<br>BIM          | <a href="#">Samples</a> |
| LMC6464BIMX      | NRND          | SOIC         | D                  | 14   | 2500           | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6464<br>BIM          |                         |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMC6464BIMX/NOPB | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | LMC6464<br>BIM          | <a href="#">Samples</a> |
| LMC6464BIN       | LIFEBUY       | PDIP         | NFF                | 14   | 25             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMC6464BIN              |                         |
| LMC6464BIN/NOPB  | ACTIVE        | PDIP         | NFF                | 14   | 25             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-NA-UNLIM     | -40 to 85    | LMC6464BIN              | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMC6462AIMX/NOPB | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| LMC6462BIMX/NOPB | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| LMC6464AIMX      | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.35    | 2.3     | 8.0     | 16.0   | Q1            |
| LMC6464AIMX/NOPB | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.35    | 2.3     | 8.0     | 16.0   | Q1            |
| LMC6464BIMX      | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.35    | 2.3     | 8.0     | 16.0   | Q1            |
| LMC6464BIMX/NOPB | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.35    | 2.3     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMC6462AIMX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6462BIMX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6464AIMX      | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6464AIMX/NOPB | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6464BIMX      | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6464BIMX/NOPB | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |

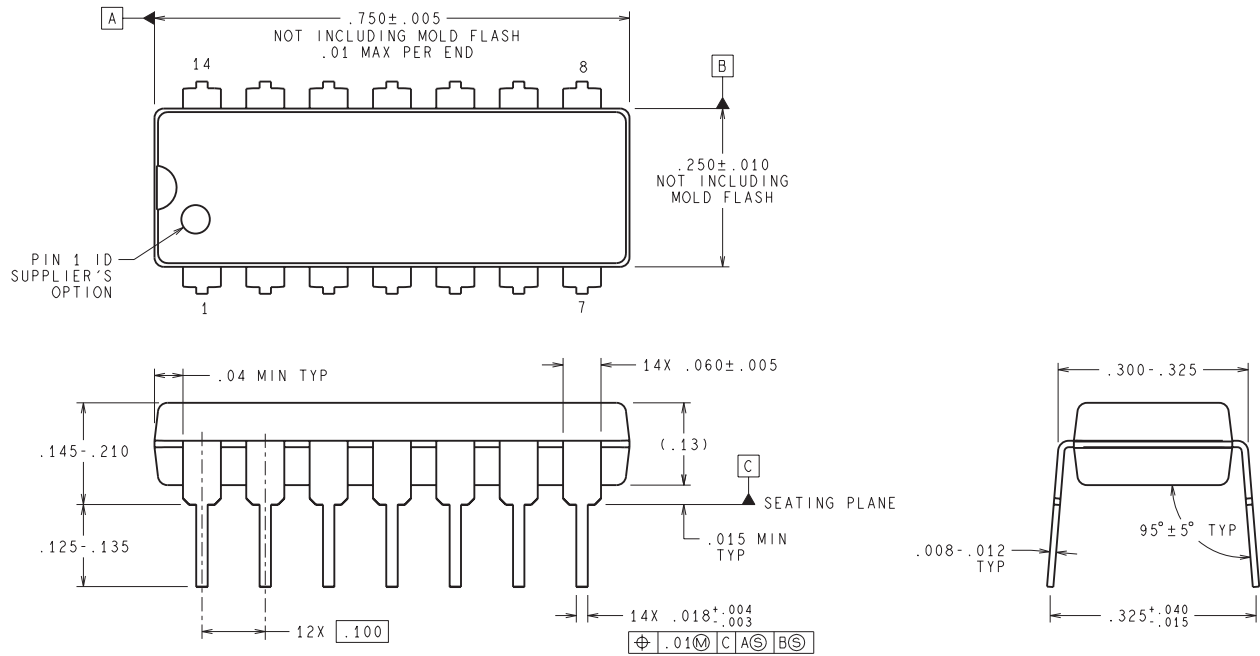
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

NFF0014A



**DIMENSIONS ARE IN INCHES**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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