3.3V to 18V Thunderbolt Power Mux

Check for Samples: TPS22981

FEATURES

- **Powered from 3.3V**
- **4.5V to 19.8V High Voltage Switch**
- **3V to 3.6V Switch**
- **Adjustable Current Limit**
- **Thermal Shutdown**
- **Make Before Break Switch**
- **High Voltage Discharge Before Low Voltage Make**
- **Reverse Current Blocking**

APPLICATIONS

- **Notebook Computers**
- **Desktop Computers**
- **Power Management Systems**

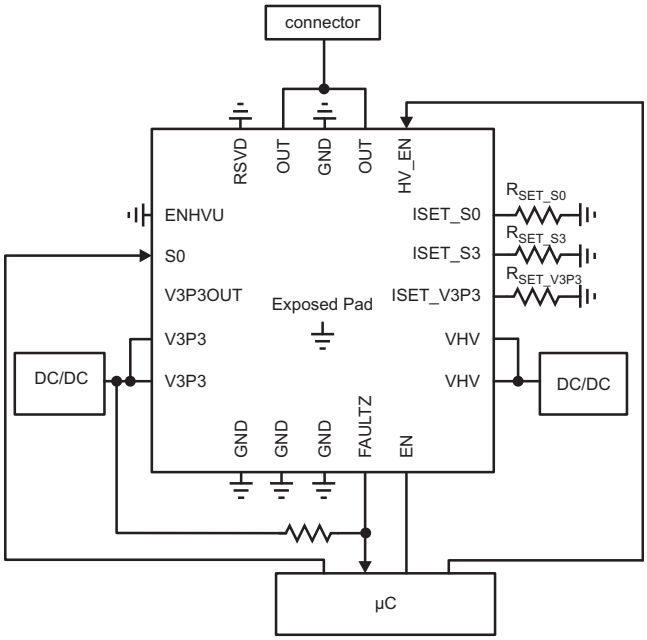


Figure 1. Typical Application

DESCRIPTION

The TPS22981 is a current-limited power mux providing a connection to a peripheral device from either a low voltage supply (3V to 3.6V) or a high voltage supply (4.5V to 19.8V). The desired output is selected by digital control signals.

The high voltage (VHV) and low voltage (V3P3) switch current limits are set with external resistance. Once the current limit is reached, the TPS22981 will control the switch to maintain the current at this limit.

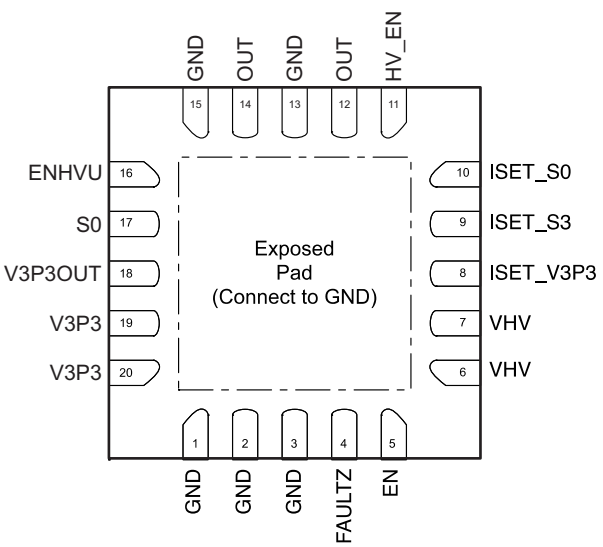
When the high voltage supply is not present, the TPS22981 will maintain the connection to the output from the low voltage supply. Upon the presence of a high voltage line and high voltage enable signal, the high voltage switch is turned on in conjunction with the low voltage switch until a reverse current is detected through the low voltage switch, allowing a seamless transition from low voltage to the high voltage supply with minimal droop and shoot-through current.

To prevent current backflow during a switch over from a VHV connection to a V3P3 connection, the TPS22981 will break the VHV connection, discharge the output to approximately 3.3V and then make the V3P3 connection. The output will transition to 0V when a load is present, before returning to 3.3V.

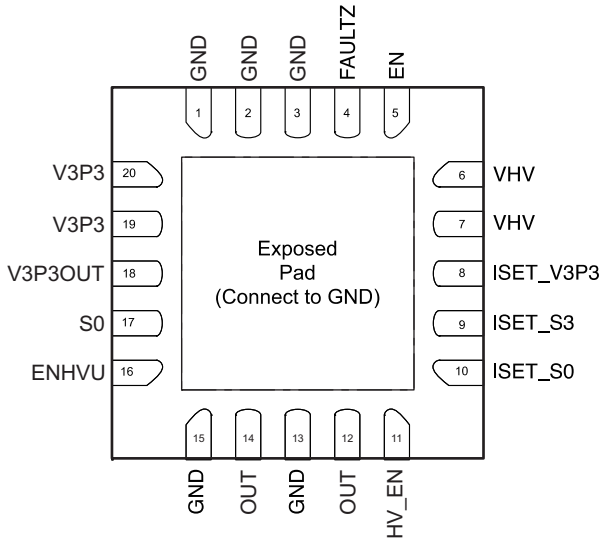
The TPS22981 is available in a 4mm x 4mm x 1mm QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Top View/Footprint



Bottom View



Package Size: 4mm x 4mm x 1mm height
Pad Pitch: 0.5mm

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE(1) θ_{JA}	POWER RATING(1) T_A = 25°C	POWER RATING(1) T_A = 70°C	DERATING FACTOR ABOVE(2) T_A = 25°C
RGP	39.3°C/W	2.16W	1.02W	25.4mW/°C

(1) Simulated with high-K board
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_I	Input voltage range on V3P3 (VDD)(2)	–0.3 to 3.6	V
	Input voltage range on EN, HV_EN, ENHVU, ISET_V3P3, ISET_S0, ISET_S3, S0(2)	–0.3 to V3P3+0.3	
	Output voltage range on FAULTZ	–0.3 to V3P3+0.3	
	Input voltage range on VHV(2)	–0.3 to 20	
	Output voltage range at OUT(2)	–0.3 to 20	
	Voltage range between VHV and OUT (V_{VHV}–V_{OUT})	–7 to 20	
	Output voltage range at V3P3OUT(2)	–0.3 to V3P3+0.3	
T_A	Operating ambient temperature range(3)	–40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	110	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD Rating	Charge Device Model (JESD 22 C101)	500	V
	Human Body Model (JESD 22 A114)	2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [TA(max)] is dependent on the maximum operating junction temperature [TJ(max)], the maximum power dissipation of the device in the application [PD(max)], and the junction-to-ambient thermal resistance of the part/package in the application (M JA), as given by the following equation: TA(max) = TJ(max) – (M JA × PD(max))

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{3P3}	Supply voltage range		3	3.6	V
V_{HV}			4.5	19.8	V
$I_{LIM3P3OUT}$	V3P3OUT Switch current range		0	500	mA
V_{IH}	Input logic high	EN, HV_EN, ENHVU, S0	V3P3-0.6	V3P3	V
V_{IL}	Input logic low	EN, HV_EN, ENHVU, S0	0	0.6	V
R_{SET_V3P3}	3.3V switch current limit set resistance		26.7	402	kΩ
R_{SET_S0}	VHV switch current limit in S0 mode set resistance		26.7	402	kΩ
R_{SET_S3}	VHV switch current limit in S3 mode set resistance		26.7	402	kΩ
R_{FAULTZ}	FAULTZ pull-up resistance to V3P3		30		kΩ

ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_J ≤ 85°C. Typical values are for V_{3P3} = 3.3V, V_{HV} = 15V, and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS						
V_{3P3}	V3P3 Input voltage range		3	3.3	3.6	V
V_{HV}	VHV Input voltage range		4.5		19.8	V
I_{VHVACT}	Active quiescent current from VHV	HV_EN = 1, EN = 1			150	µA
I_{VHVSD}	Shutdown leakage current from VHV	HV_EN = 0, EN = 0 or 1			60	µA
I_{DDACT}	Active quiescent current from V3P3	EN = 1, HV_EN = 0			500	µA
$I_{DDACTHV}$		EN = 1, HV_EN = 1			500	µA
I_{DDSD}	Shutdown quiescent current from V3P3	EN = 0, OUT = 0 V			30	µA
I_{DIS}	OUT Discharge current	EN = 1, V_{HV} = 5V, HV_EN = 1→0	5		10	mA
I_{IN}	HV_EN, EN, ENHVU, S0, S3 Input pin leakage	V = 0 V			1	µA
		V = V3P3			1	
SWITCH AND RESISTANCE CHARACTERISTICS						
R_{SHV}	VHV Switch resistance	V_{HV} = 5V to 18V, I_{VHV} = 0.9A			250	mΩ
R_{S3P3}	V3P3 Switch resistance	V_{3P3} = 3.3 V, I_{V3P3} = 0.9 A			125	mΩ
$R_{S3P3BYP}$	V3P3 Bypass switch resistance	V_{3P3} = 3.3 V, I_{V3P3} = 500 mA			500	mΩ
R_{OUTDIS}	OUT Pulldown resistance when disabled	EN = 0	1.5	2.5	4	kΩ
$V_{OLFAULTZ}$	FAULTZ VOL	I_{FAULTZ} = 250 µA			0.6	V
VOLTAGE THRESHOLDS						
V_{HVUVLO}	VHV Under voltage lockout	VHV Input falling	3.6	4		V
		VHV Input rising		4	4.3	
$V_{3P3UVLO}$	V3P3 Under voltage lockout	V3P3 Input falling	1.8	2.25		V
		V3P3 Input rising		2.25	2.5	
$V_{FAULTZVAL}$	V3P3 Voltage for valid FAULTZ	EN = 1	1.8			V
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature		110	120	130	°C
T_{SDHYST}	Shutdown hysteresis			10		°C
CURRENT LIMIT						
I_{LIMHV}	VHV Switch current limit state S0 or S3	$R_{SET\_S0,3}$ = 402 kΩ(1)	80	100	120	mA
		$R_{SET\_S0,3}$ = 80.6 kΩ(1)	446	496	546	
		$R_{SET\_S0,3}$ = 26.7 kΩ(1)	1423	1498	1573	
$I_{LIMVHVMAX}$	Maximum VHV switch current limit	$R_{SET\_S0,3}$ = 0 Ω	1.8	2.4	3.1	A
I_{LIM3P3}	V3P3 Switch current limit	R_{SET_V3P3} = 402 kΩ(1)	80	100	120	mA
		R_{SET_V3P3} = 80.6 kΩ(1)	446	496	546	
		R_{SET_V3P3} = 26.7 kΩ(1)	1423	1498	1573	
$I_{LIM3P3MAX}$	Maximum V3P3 switch current limit	R_{SET_V3P3} = 0Ω	1.8	2.4	3.1	A
I_{REV3P3}	V3P3 Switch reverse current limit		10	40	85	mA
T_{V3P3RC}	V3P3 Switch reverse current response time	V_{OUT} = V_{3P3}→V_{3P3} + 20 mV			100	µs
T_{VHVSC}	VHV Switch short circuit response time	C_{OUT} ≤ 20 pF		8		µs
T_{V3P3SC}	V3P3 Switch short circuit response time	C_{OUT} ≤ 20 pF		8		µs
TRANSITION DELAYS						
T_{3P3OFF}	VHV to V3P3 Off time	C_{OUT} = 1.1 µF, EN = 1, HV_EN = 1→0			6	ms
$T_{0\text{-}3.3V}$	0V to 3.3V Ramp time	C_{OUT} ≤ 20 pF			6	ms
$T_{3.3V\text{-}VHV}$	3.3V to VHV Ramp time	C_{OUT} ≤ 20 pF			6	ms
$T_{VHV\text{-}3.3V}$	VHV to 3.3V Ramp time	C_{OUT} ≤ 20 pF			23	ms
T_{LIM}	Overcurrent response time	C_{OUT} ≤ 20 pF, I_{OUT} = 6 A			0.5	ms

(1) Equation 1 is used to calculate the required resistance for a given minimum I_{LIM}. The nearest 1% resistance is chosen and the corresponding I_{LIM} variance is shown.

FUNCTIONAL BLOCK DIAGRAM

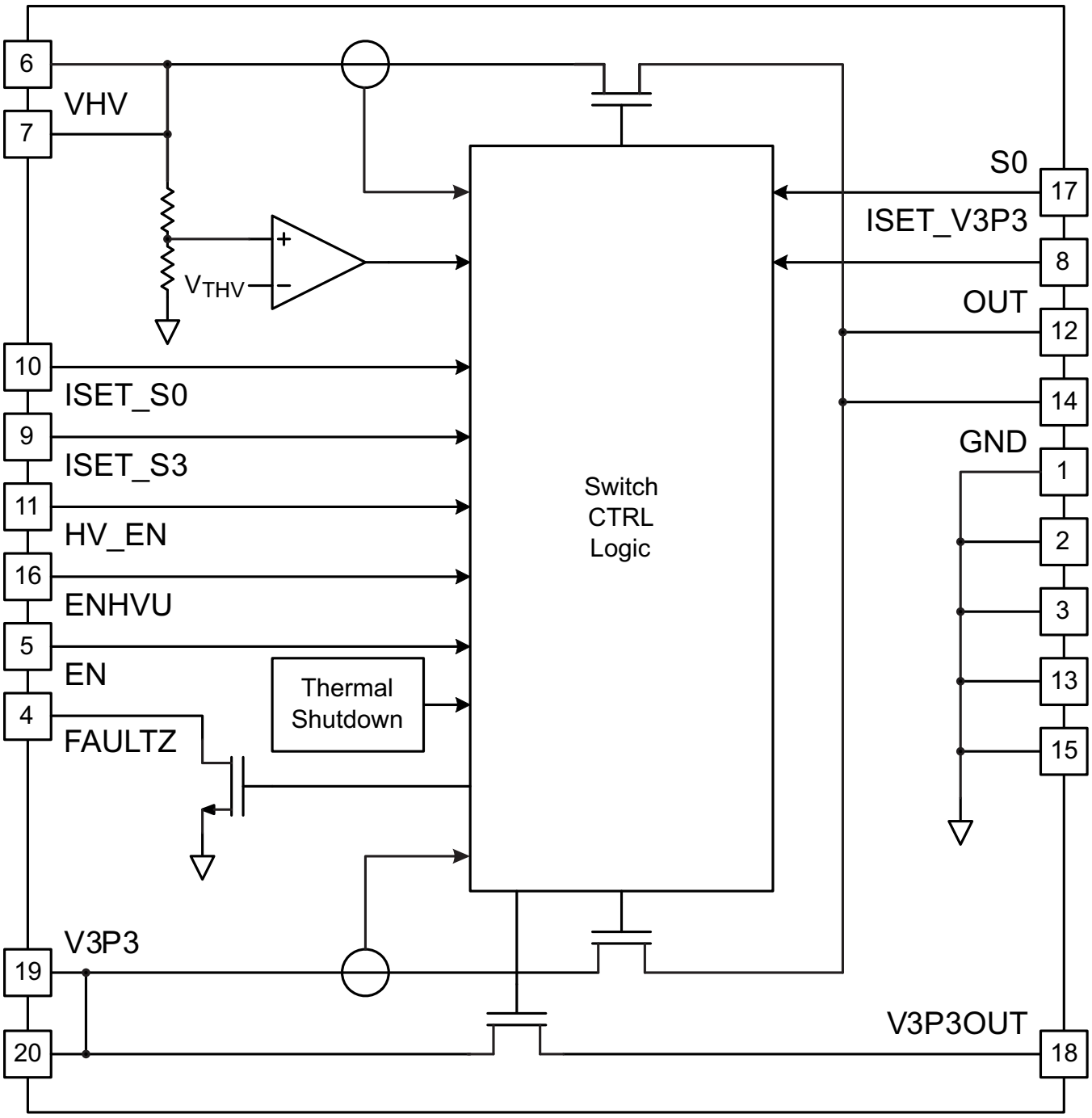


Figure 2. Functional Block Diagram

PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1, 2, 3, 13, 15	GND	Device ground. All GND pins must be connected to board ground.
4	FAULTZ	Fault condition output. This pin is an open drain pull-down indicating a fault condition. Place a pull-up resistance (R_{FAULTZ}) between this pin and V3P3. Float pin or tie pin to GND if unused.
5	EN	Device active-high enable.
6, 7	VHV	High voltage power supply input. See the Input Inductive Bounce at Short Circuit section for more information.
8	ISET_V3P3	Sets the current limit for V3P3. Place resistor between this pin and GND. See Equation 3 to calculate resistor value.
9	ISET_S3	Sets the current limit for VHV in S3 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
10	ISET_S0	Sets the current limit for VHV in S0 mode. Place resistor between this pin and GND. See Equation 2 to calculate resistor value.
11	HV_EN	Active-high voltage output enable.
12, 14	OUT	Power output. Place a minimum of 1µF capacitor as close to this pin as possible.
16	ENHVU	Enable VHV UVLO control of device enable. When asserted high, both V3P3 and VHV must be present for device enable. When low, only V3P3 must be present for device enable.
17	S0	When this pin is asserted, the device is put in S0 mode. Otherwise the device operates in S3 mode.
18	V3P3OUT	3.3V bypass output. When ENHVU is low, this path is enabled by EN and the V3P3 UVLO. When ENHVU is high, this path is enabled by EN and both the V3P3 UVLO and the VHV UVLO. Place a minimum of 0.1µF capacitor as close to this pin as possible.
19, 20	V3P3	3.3V power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.
EP	GND	Exposed pad must be connected to device GND.

APPLICATION INFORMATION

TYPICAL APPLICATION

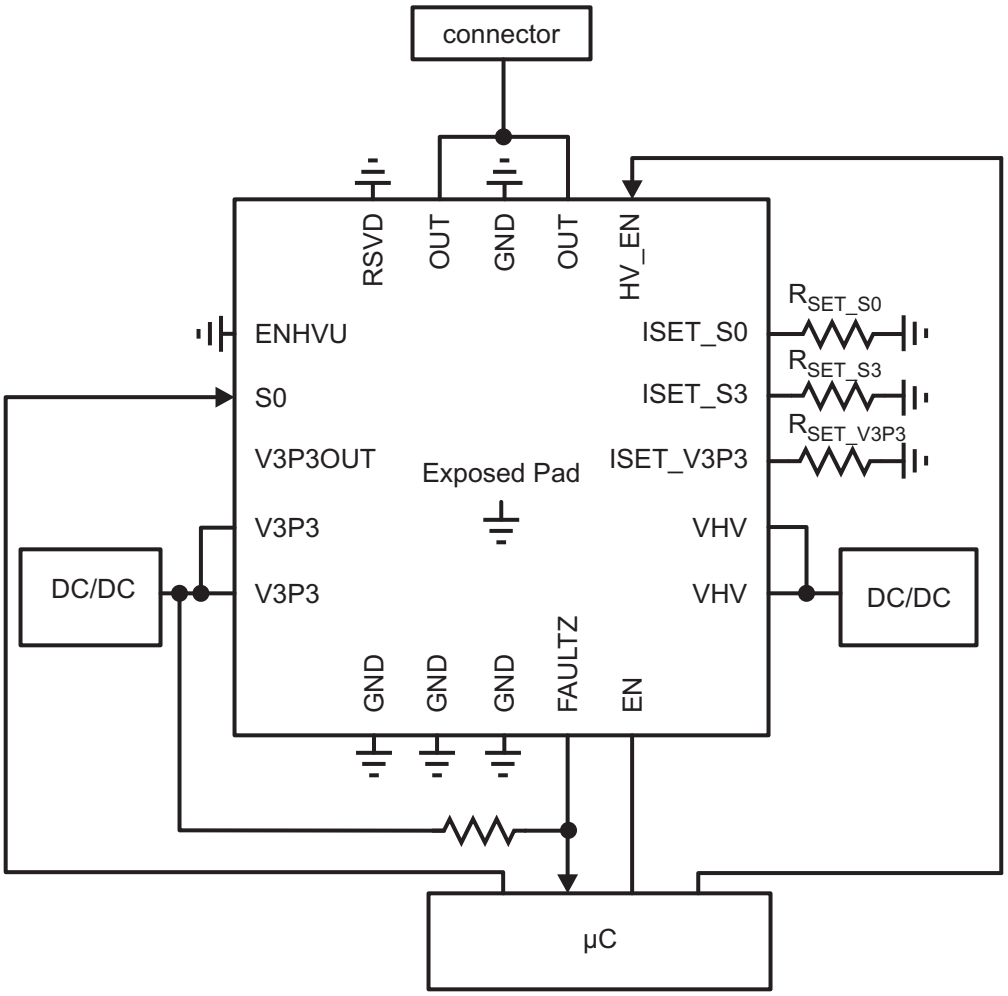


Figure 3. Typical Application

CURRENT LIMIT

Figure 4 shows a simplified view of the TPS22981 current limit function. Both the high voltage supply current limit and the V3P3 supply current limit are adjustable by external resistors

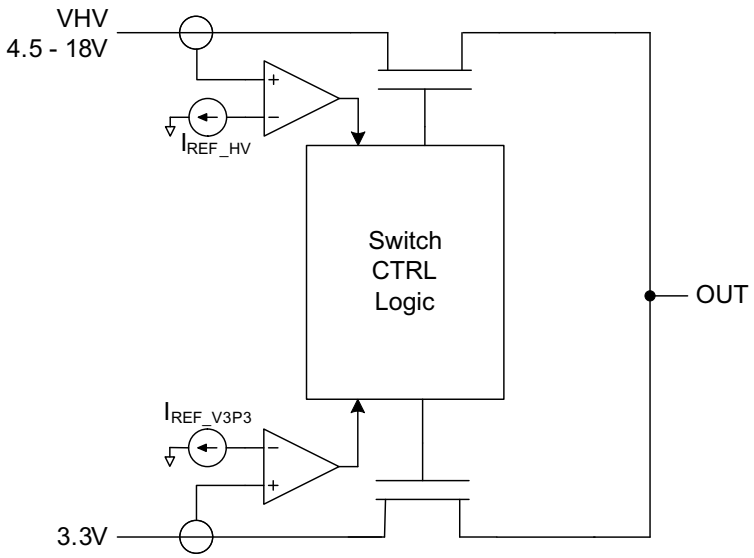


Figure 4. Simplified Current Limit Diagram

The current I_{REF_HV} and I_{REF_V3P3} that set the current limit threshold are set with three external resistors as shown in Figure 5. When the TPS22981 is passing the V3P3 voltage, the current limit is set by R_{SET_V3P3}. The VHV path has two modes that allow setting two different current limits. The S0 pin determines which current limit is used. When S0 is asserted high, R_{SET_S0} sets the current limit. When S0 is low, R_{SET_S3} sets the current limit. This allows the system to have two separate VHV current limits for different modes such as active and sleep.

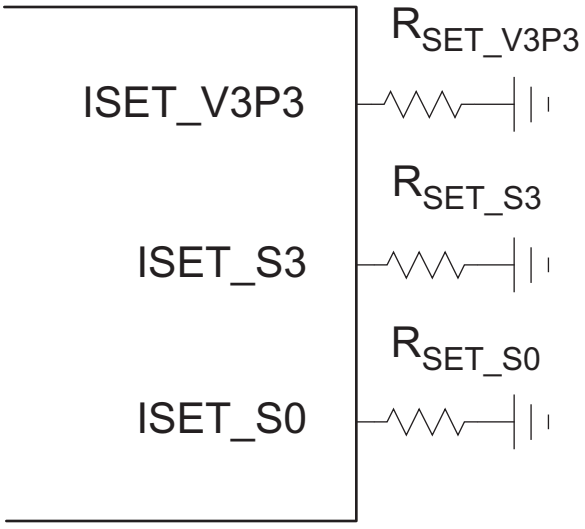


Figure 5. External R_{SET} Resistance to set Current Limits

CURRENT LIMIT THRESHOLD

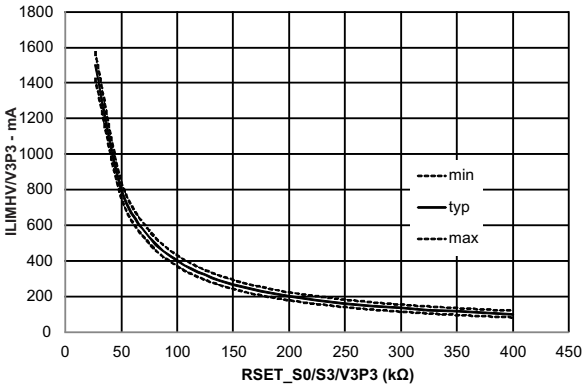


Figure 6. I_{LIM} vs R_{SET} for VHV and V3P3

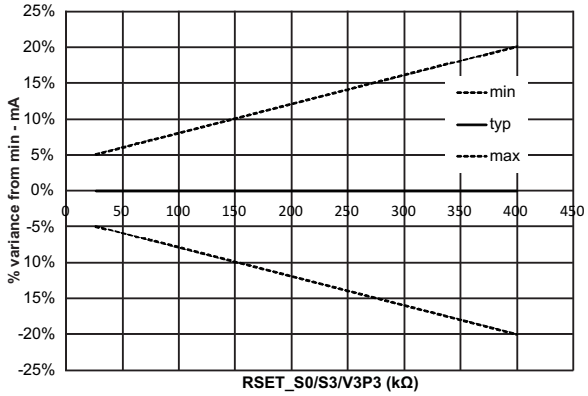


Figure 7. % Variance from min I_{LIM} vs R_{SET}

Figure 6 shows the minimum, typical, and maximum current limit for either supply versus its corresponding R_{SET} value. Equation 1 is used to determine the RSET needed to set a typical I_{LIM} for a given supply and mode. Figure 7 shows the percent variation from the typical I_{LIM} value to the minimum and maximum I_{LIM} values.

$$R_{SET} = \frac{40\ k\Omega \times Amps}{I_{LIMTYP}} \quad (1)$$

Where

R_{SET} = external resistor used to set the current limit for V3P3, VHV (S0), or VHV (S3), and
I_{LIMTYP} = typical current limit for V3P3, VHV (S0), or VHV (S3) set by the external R_{SET} resistor.

Each resistor is placed between the corresponding ISET pin and GND, as shown in Figure 5, providing a minimum current limit between 100mA and 1.5A. For a given R_{SET} the minimum current limit and the maximum current limit are determined by Equation 2 and Equation 3.

$$I_{LIMMIN} = \frac{38429}{R_{SET}} - 0.0161\ A \quad (2)$$

$$I_{LIMMAX} = \frac{41571}{R_{SET}} + 0.0161\ A \quad (3)$$

MAXIMUM CURRENT LIMIT THRESHOLD

The TPS22981 has a maximum current limit $I_{LIMVHVMAX}$ and $I_{LIM3P3MAX}$. This prevents excessive current in the case of an ISET pin being shorted to ground.

TRANSITION DELAYS

Output transitions of the TPS22981 voltages are shown in Figure 8. When the device transitions from V_{HV} to V_{3P3} at the output, the power switches both turn off until the output falls to near the V_{3P3} voltage. During this time, a discharge current of I_{DIS} pulls OUT down. If a load is also pulling current from OUT, the output will drop to near 0V due to the switch off time of T_{3P3OFF}.

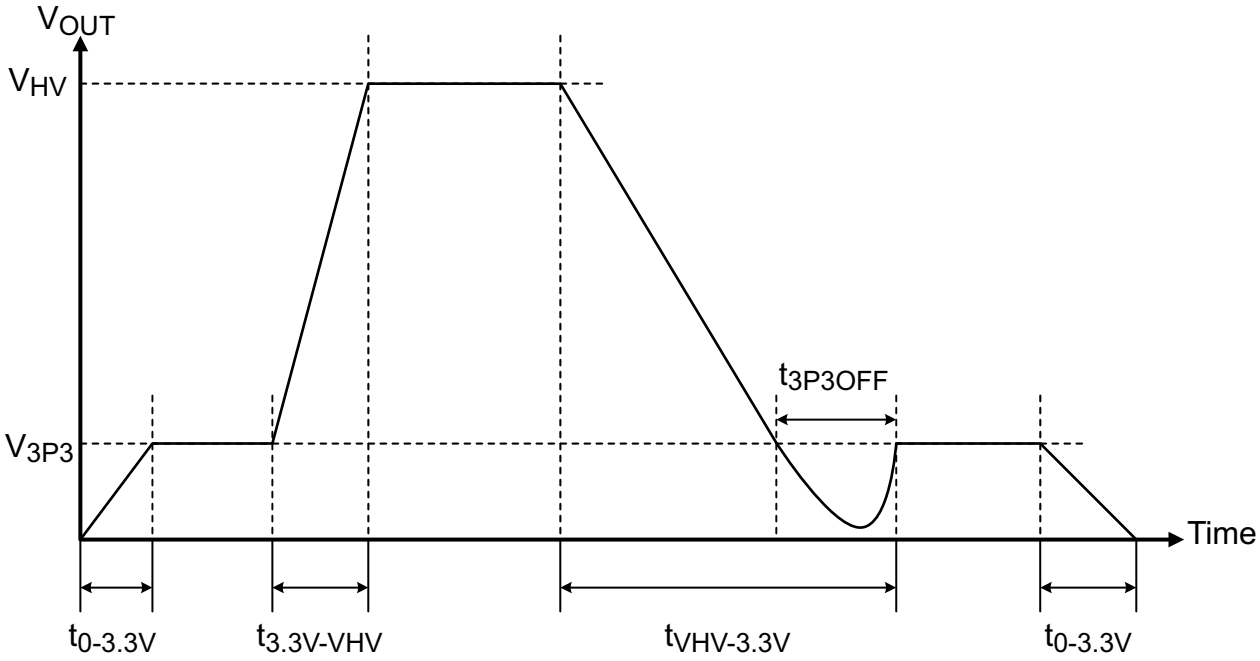


Figure 8. Output Voltage Transitions (Timing transitions are 10% to > 90%)

DIGITAL CONTROL SIGNALS

The voltage at OUT is controlled by two input digital logic signals, EN and HV_EN. HV_EN controls the state of the VHV switch and EN controls the state of V3P3 switch. Table 1 lists the possible output states given the conditions of the digital logic signals and the device is not in UVLO. See Table 2 for a more complete description including both UVLO conditions.

Table 1. Output state of OUT Given the States EN and HV_EN

EN	HV_EN	OUT
0	0	OPEN
0	1	OPEN
1	0	V3P3
1	1	VHV

Figure 9 shows possible combinations of EN and HV_EN controlling OUT of the TPS22981.

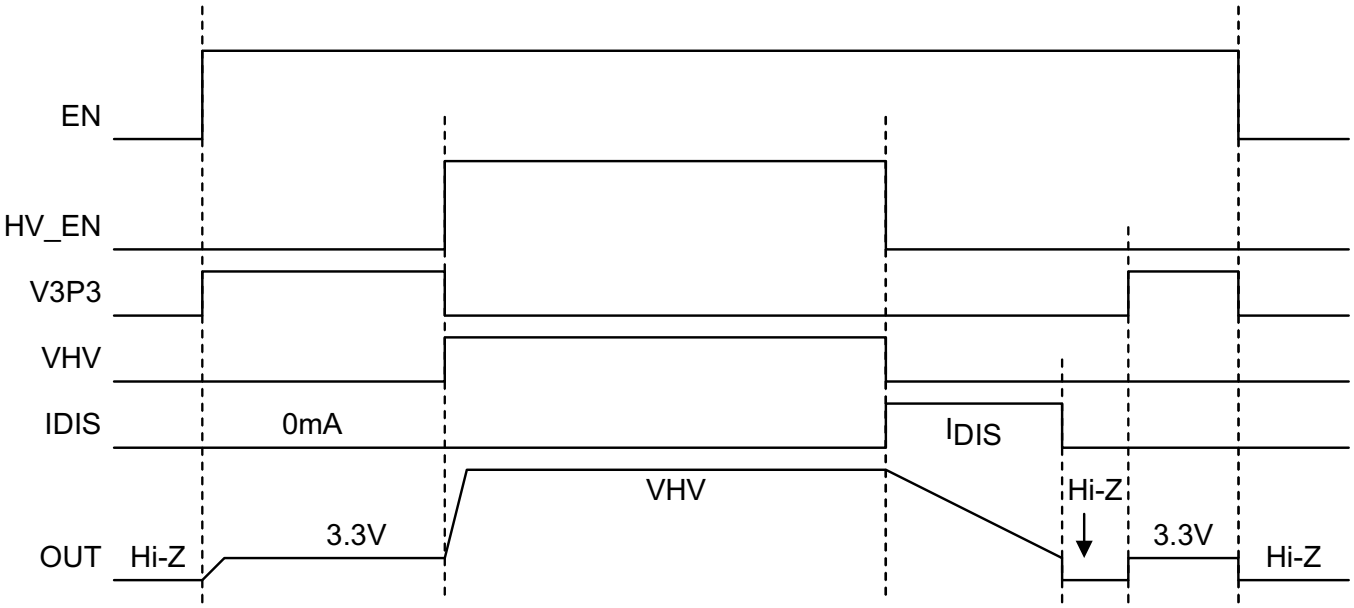


Figure 9. Logic Waveforms Displaying the Transition Between VHV and V3P3

OVER-CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

When the load at OUT attempts to draw more current than the limit set by the external R_{SET} resistors for the V3P3 switch and VHV switch (for both S0 and S3 modes), the device will operate in a constant current mode while lowering the output voltage. Figure 10 shows the delay, t_{LIM}, which occurs from the instance an over-current fault is detected until the output current is lowered to I_{LIMHV} tolerances for VHV or I_{LIM3V3} tolerances for V3P3 shown in Figure 6. Figure 11 shows the response time versus a resistance shorted across the output.

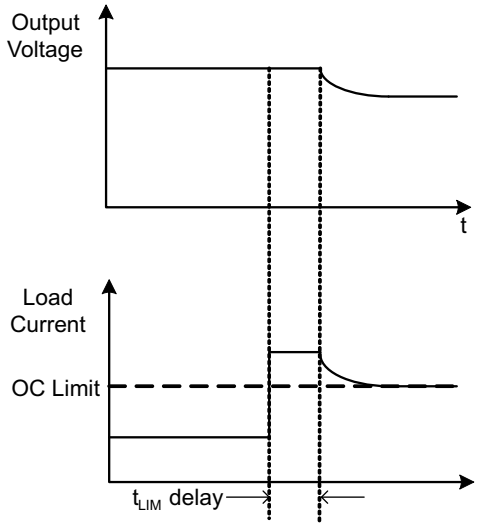


Figure 10. Overcurrent Output Response

Figure 11. Overcurrent Response Time vs Short Resistance

All short circuit conditions are treated as over-current conditions. In the event of a short circuit, the device will limit the output current to the corresponding R_{SET} value and continue to do so until thermal shutdown is encountered or the short circuit condition is removed.

REVERSE CURRENT PROTECTION

Reverse current protection for the V3P3 supply to OUT triggers at I_{REV3P3} causing the V3P3 supply switch to open. When the HV_EN signal is not asserted and reverse current protection is triggered, a discharge current source is turned on to bring the output voltage to near the V3P3 voltage.

REVERSE CURRENT BLOCKING

The VHV switch blocks reverse current flow from OUT to VHV when the switch is off.

THERMAL SHUTDOWN

The device enters thermal shutdown when junction temperature reaches T_{SD}. The device will resume previous state on power up once the junction temperature has dropped by 10C. Connect thermal vias to the exposed GND pad underneath the device package for improved thermal diffusion.

UVLO and ENABLE

When ENHVU is low, the TPS22981 is enabled by the logical AND of the EN input, the V3P3 UVLO, and the Thermal Shutdown. When the V3P3 UVLO threshold has been crossed, the device is not in thermal shutdown, and the EN input is high, the device will enable. When the V3P3 UVLO triggers, regardless of the states of any digital logic controls, the device will open all switches.

ENHVU adds the VHV UVLO to the logical decision enabling the device. When ENHVU is high, the TPS22981 is enabled by the logical AND of the EN input, the V3P3 UVLO, the VHV UVLO, and the Thermal Shutdown. When both UVLO thresholds have been crossed, the device is not in thermal shutdown, and the EN input is high, the device will enable. When either UVLO triggers, regardless of the states of any digital logic controls, the device will open all switches. Table 2 shows the pin and voltage configurations for enabling the device. Note, a 1 for the UVLO columns means the device is in a UVLO condition. A PD indicates a pulldown resistance of R_{OUTDIS} to GND.

Table 2. Device Enable Control (when in an under-voltage condition, UVLO = 1)

EN	ENHVU	HV_EN	V3P3 UVLO	VHV UVLO	OUT
0	X	X	X	X	PD
1	X	X	1	X	PD
1	1	X	0	X	OPEN
1	1	X	1	X	PD
1	0	0	0	X	V3P3
1	1	0	0	0	V3P3
1	X	1	0	0	VHV
1	0	1	0	1	V3P3

FAULTZ Output

The TPS22981 has an open-drain FAULTZ output. When the device is in a fault condition, the FAULTZ output will pull low. Connect FAULTZ through a pull-up resistance to V3P3. A Fault occurs during any of the following conditions.

- EN = 1 and V3P3 is in UVLO (device enabled and V3P3 is in an under-voltage condition)
- EN = 1 and in Thermal Shutdown condition
- EN = 1, HV_EN = 1, and VHV is in UVLO (device enabled, high voltage enabled, and VHV is in an under-voltage condition)

Table 3 shows these conditions and the resulting FAULTZ output. Note, when V3P3 is below the UVLO threshold, FAULTZ will be 0 when EN=1 or 1 when EN=0. However, when V3P3 falls below $V_{FAULTZVAL}$, the FAULTZ output is unknown.

Table 3. FAULTZ Output Conditions (when in an under-voltage condition, UVLO = 1)

EN	HV_EN	Thermal Shutdown	V3P3 UVLO	VHV UVLO	FAULTZ (Active Low)
0	X	X	X	X	1
1	X	X	1	X	0
1	X	Yes	0	X	0
1	0	No	0	1	1
1	1	No	0	1	0
1	X	No	0	0	1

It is recommended that the pull-up resistance on FAULTZ be 100kΩ and must be greater than or equal to 30kΩ.

INPUT INDUCTIVE BOUNCE AT SHORT CIRCUIT

When a significant inductance is seen at the VHV input, suddenly turning off large current through the device may produce a large enough inductive voltage bounce on the VHV pin to exceed the maximum safe operating condition and damage the TPS22981. To prevent this, reduce any inductance at the VHV input.

REVISION HISTORY

Changes from Original (December 2012) to Revision A **Page**

- Removed ordering information table. 2
- Added R_{OUTDIS} parameter to the Electrical Characteristics table. 4
- Updated UVLO ENABLE section. 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22981RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22981	Samples
TPS22981RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22981	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

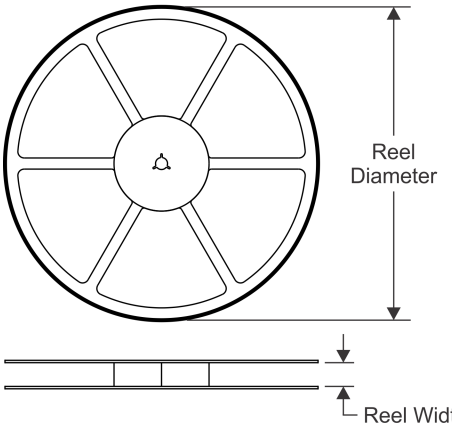
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

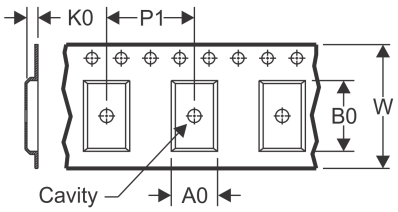
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

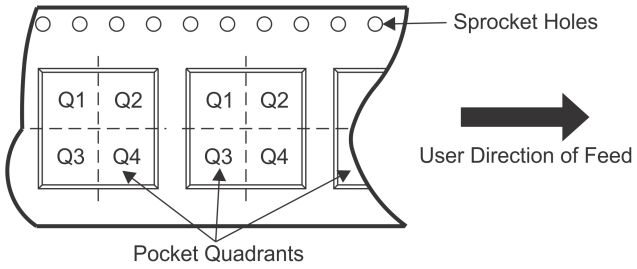


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

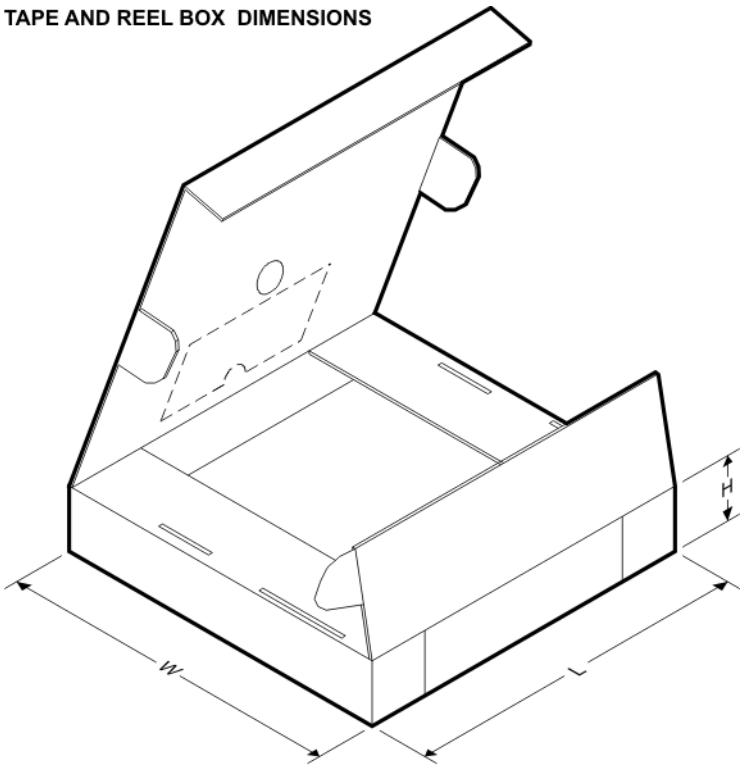
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22981RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS22981RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

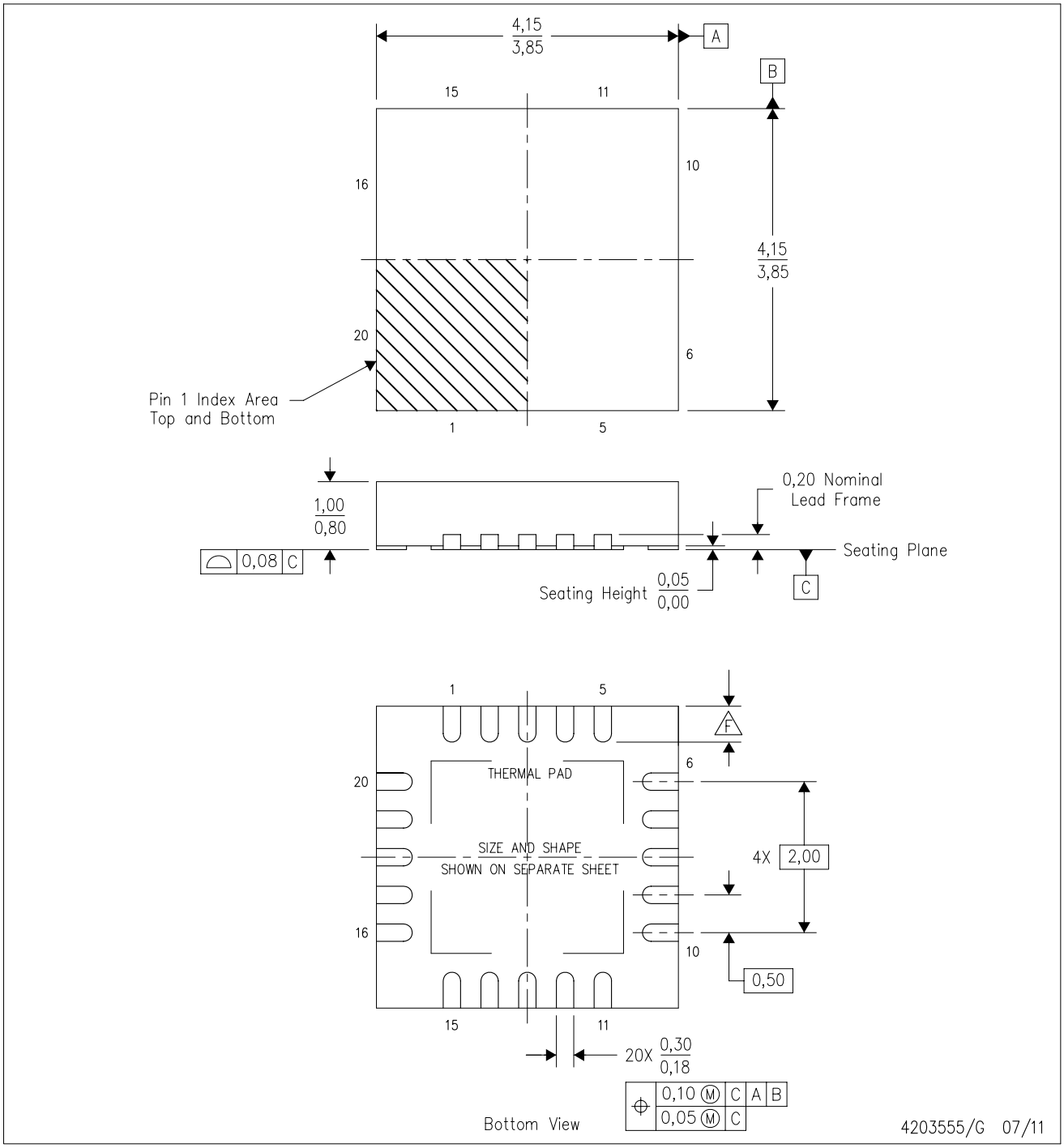
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22981RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
TPS22981RGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

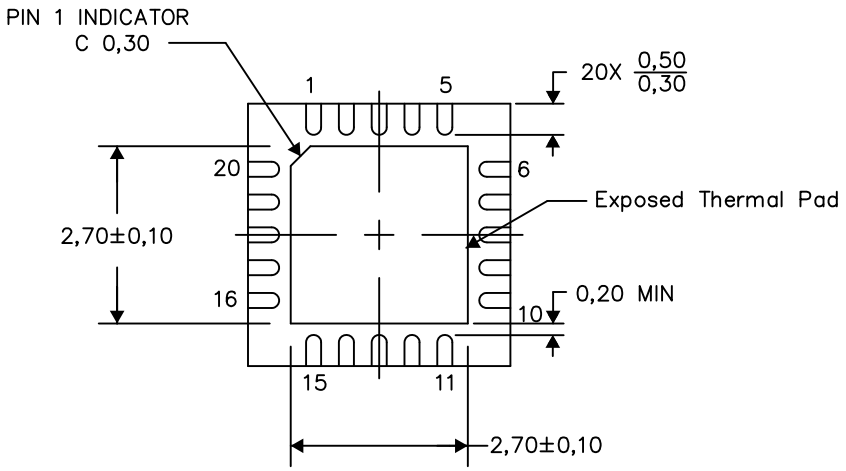
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



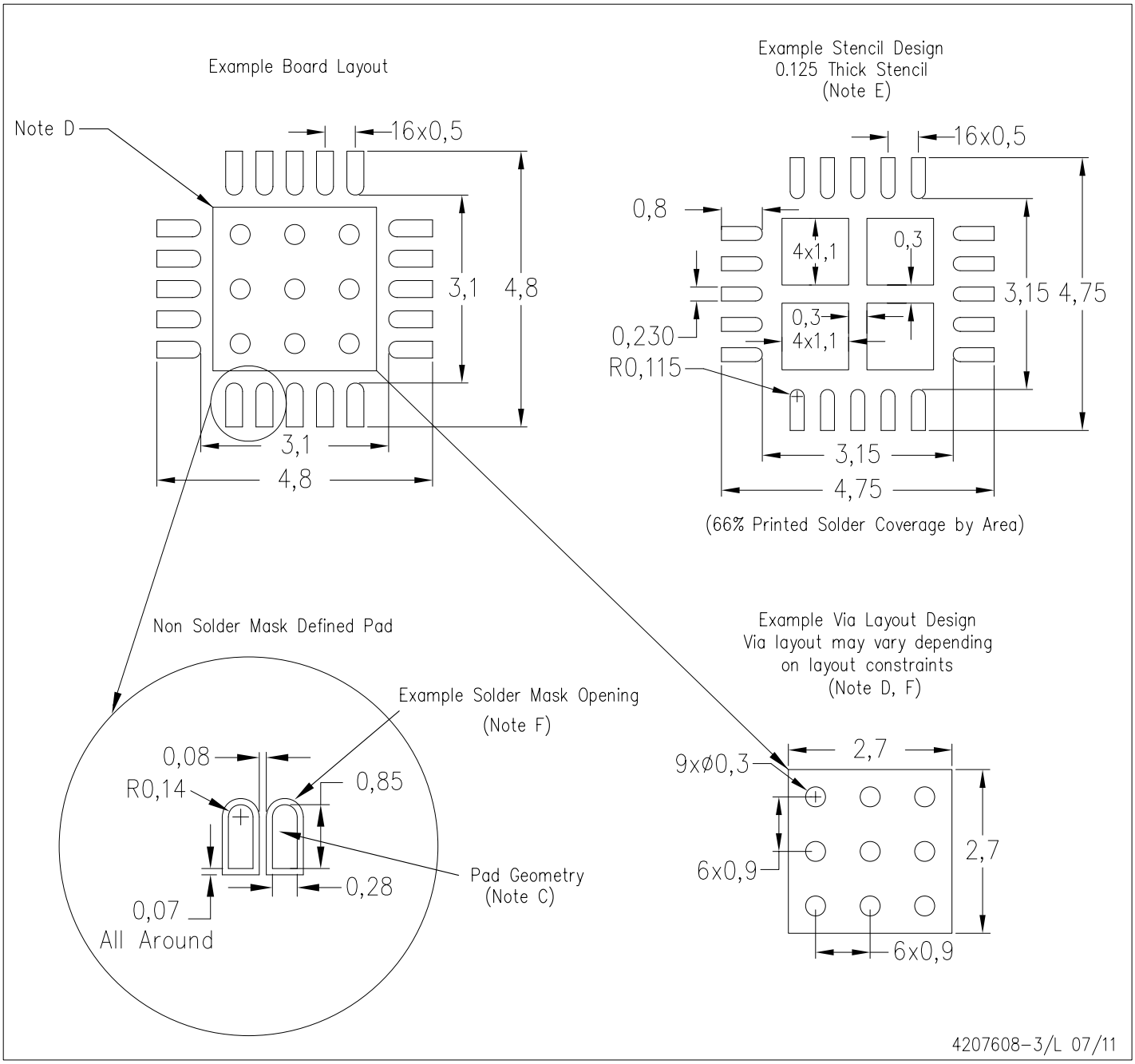
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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