



General Description

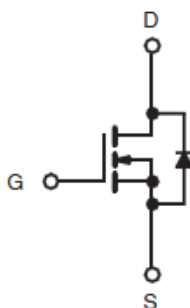
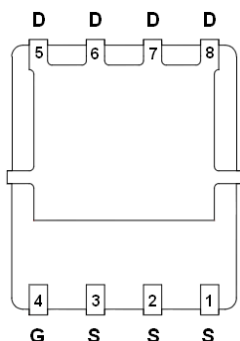
AFN6882S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 100V/20A, $R_{DS(ON)}=9m\Omega@V_{GS}=10V$
- 100V/15A, $R_{DS(ON)}=13m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- DFN5X6-8L package design

Pin Description (DFN5X6-8L)



Application

- Networking / Telecom / Server
- LED Lighting Applications
- Quick Charger Applications
- DC-DC Primary Side Switch

Pin Define

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN6882SFN568RG	6882S	DFN5X6-8L	Tape & Reel	2500 EA

- ※ A Lot code
- ※ B Date code
- ※ AFN6882SFN568RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_{DSM}	$T_A=25^\circ\text{C}$	17
		$T_A=70^\circ\text{C}$	13
Pulsed Drain Current	I_{DM}	80	A
Continuous Source Current(Diode Conduction)	I_S	4.9	
Single Pulse Avalanche Current	I_{AS}	$L=0.1\text{mH}$	30
			E_{AS}
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	5.4
		$T_A=75^\circ\text{C}$	3.4
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	$t \leq 10\text{ s}$	15
		Steady-State	45

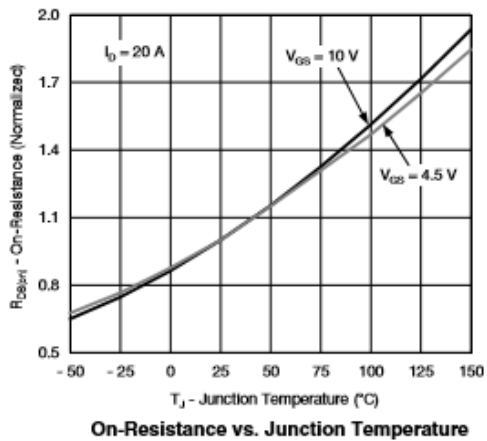
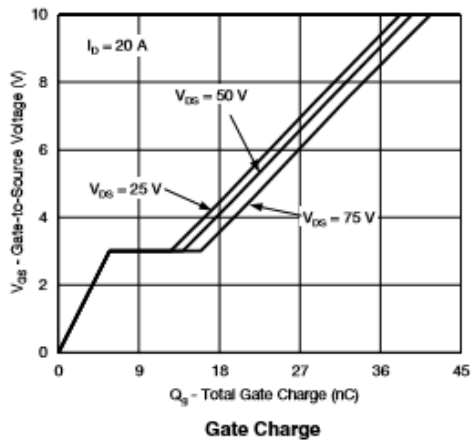
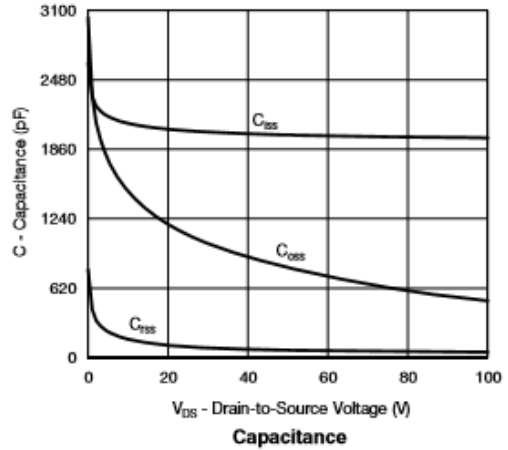
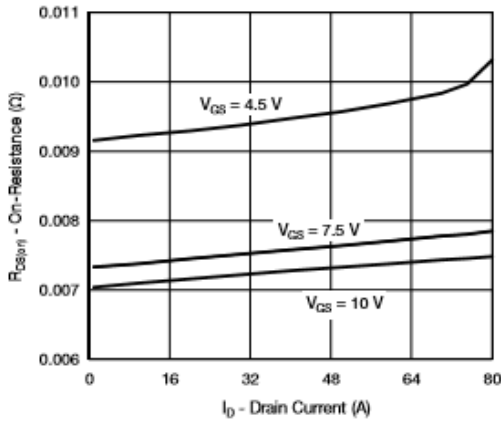
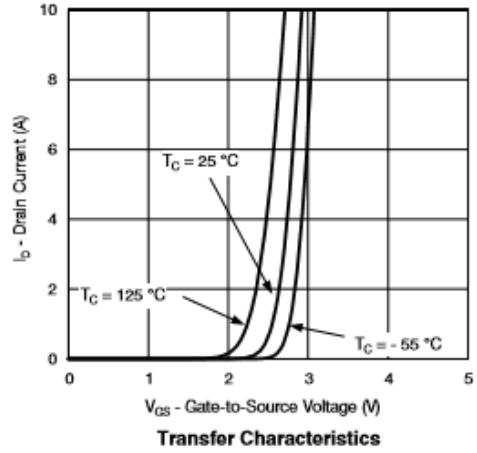
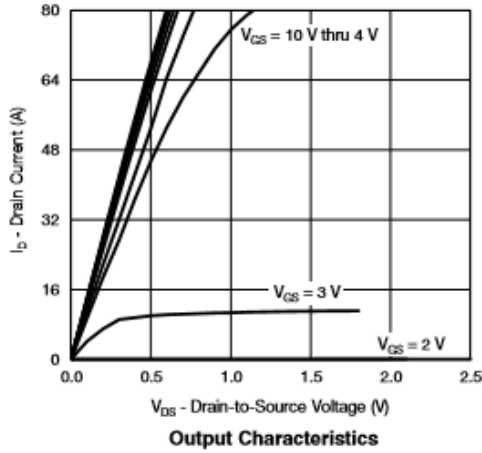
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.2		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		7.3	9	m Ω
		$V_{GS}=4.5V, I_D=10A$		10.8	13	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=20A$		60		S
Diode Forward Voltage	V_{SD}	$I_S=5A, V_{GS}=0V$		0.8	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=50V, V_{GS}=4.5V$ $I_D \equiv 10A$		20	40	nC
Gate-Source Charge	Q_{gs}		6			
Gate-Drain Charge	Q_{gd}		9			
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V$ $f=1\text{MHz}$		1950		pF
Output Capacitance	C_{oss}		735			
Reverse Transfer Capacitance	C_{rss}		60			
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=5\Omega$ $I_D \equiv 10A, V_{GEN}=10V$ $R_G=1\Omega$		12	25	ns
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			35	70	
	t_f			10	20	

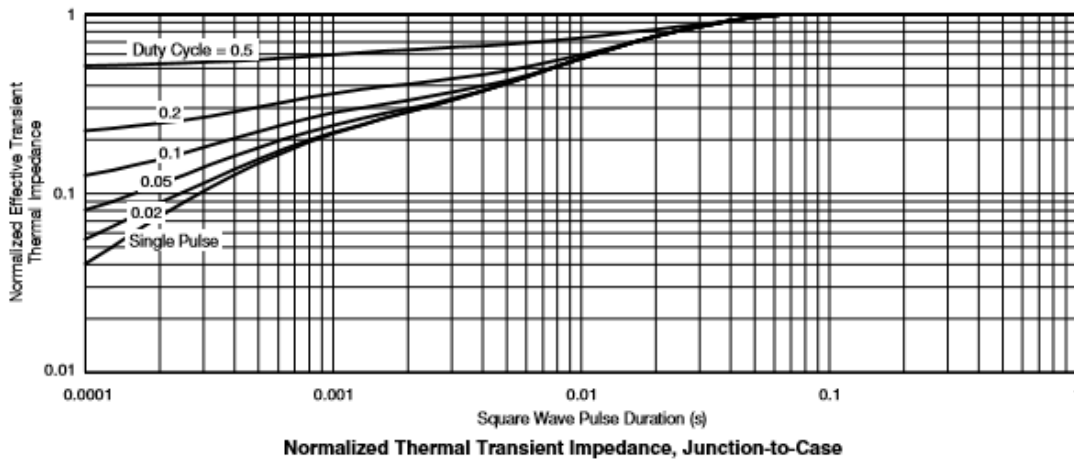
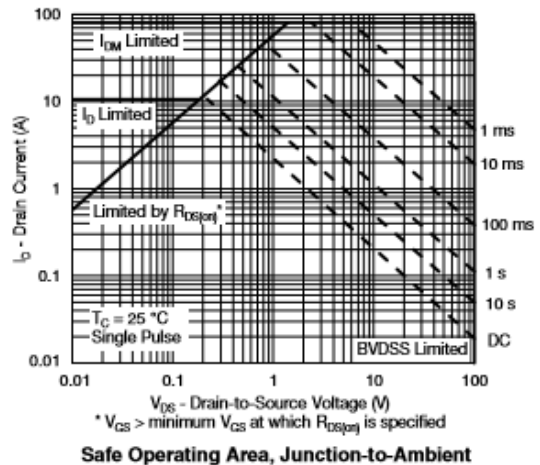
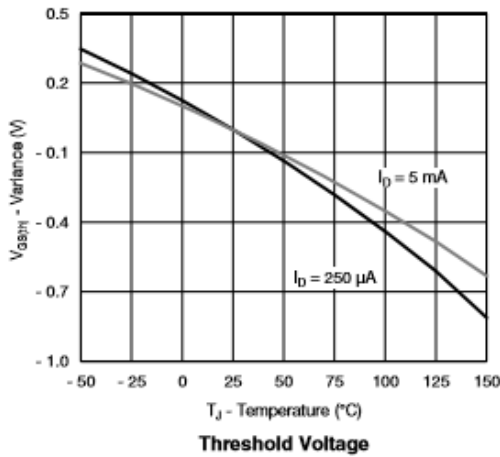
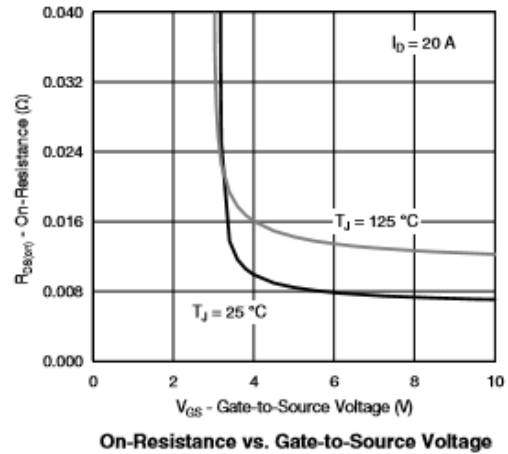
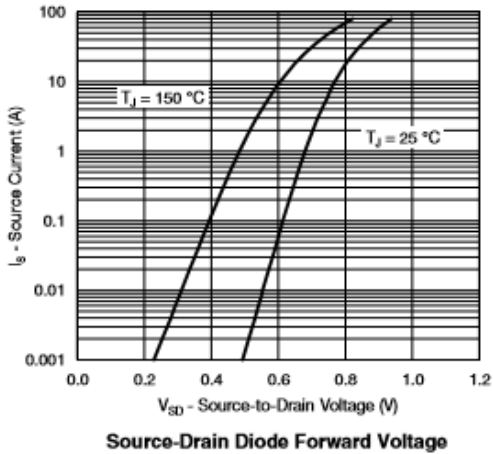


Typical Characteristics





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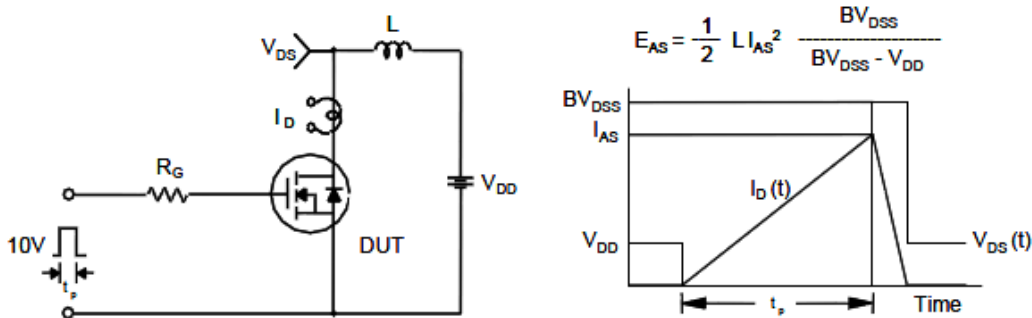
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

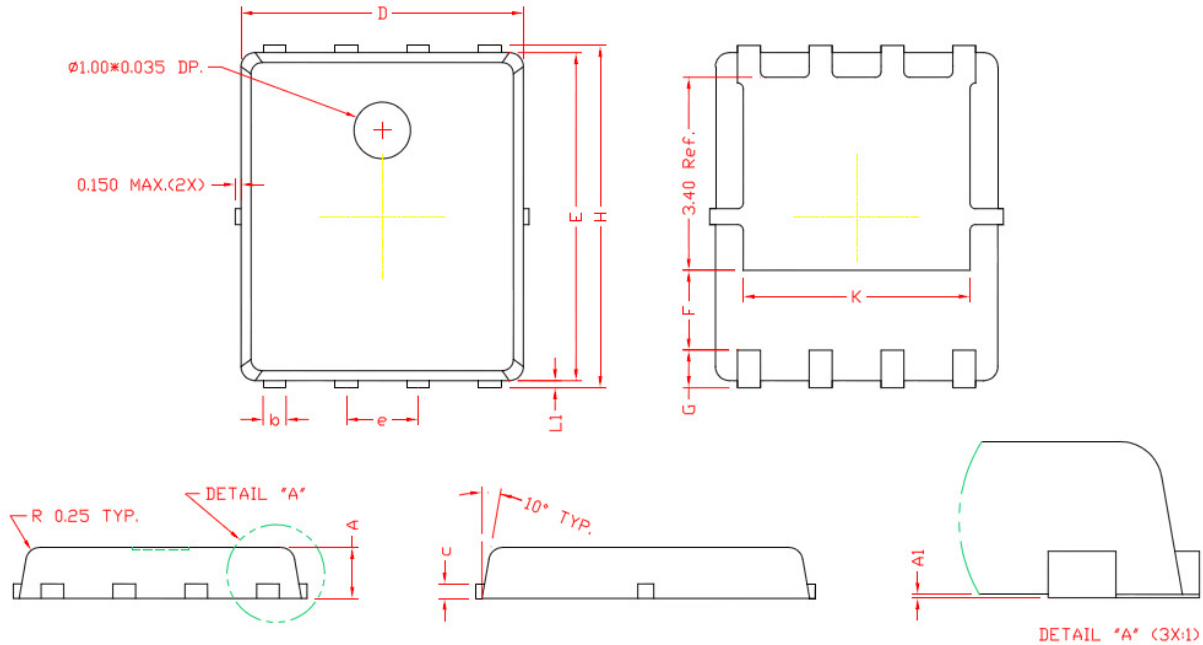


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (DFN5X6-8L)



DIMENSIONS

REF.	Millimeters		REF.	Millimeters	
	Min.	Max.		Min.	Max.
A	0.80	1.00	E	5.70	5.90
A1	0.00	0.05	e	1.27 BSC.	
b	0.35	0.49	H	5.95	6.20
c	0.254 Ref.		L1	0.10	0.18
D	4.90	5.10	G	0.60 Ref.	
F	1.40 Ref.		K	4.00 Ref.	

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