

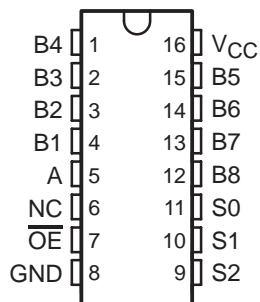
# SN74CBTLV3251

## LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMUTIPLEXER

SCDS054I – MARCH 1998 – REVISED OCTOBER 2003

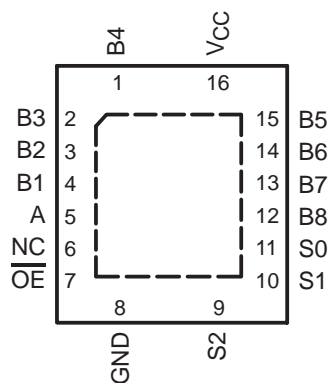
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

D, DBQ, DGV, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

RGY PACKAGE  
(TOP VIEW)



NC – No internal connection

### description/ordering information

The SN74CBTLV3251 device is a 1-of-8 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select inputs (S0, S1, S2) control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ( $\overline{OE}$ ) input is high.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

| $T_A$         | PACKAGE†          |                   | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|-------------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY         | Tape and reel     | SN74CBTLV3251RGYR     | CL251            |
|               | SOIC – D          | Tube              | SN74CBTLV3251D        | CBTLV3251        |
|               |                   | Tape and reel     | SN74CBTLV3251DR       |                  |
|               | SSOP (QSOP) – DBQ | Tape and reel     | SN74CBTLV3251DBQR     | CL251            |
|               | TSSOP – PW        | Tape and reel     | SN74CBTLV3251PWR      | CL251            |
| TVSOP – DGV   | Tape and reel     | SN74CBTLV3251DGVR | CL251                 |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

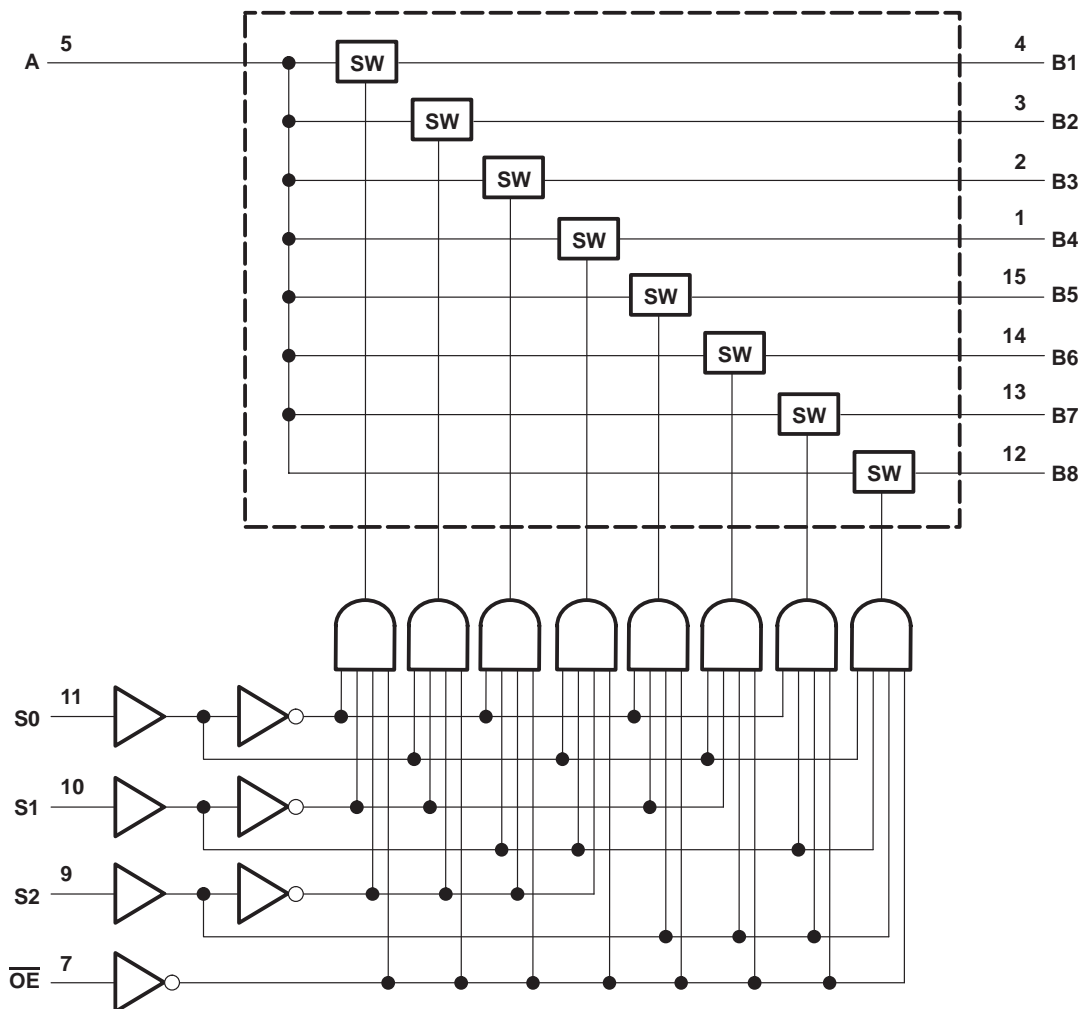
# SN74CBTLV3251 LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS054I – MARCH 1998 – REVISED OCTOBER 2003

FUNCTION TABLE

| INPUTS          |    |    |    | FUNCTION         |
|-----------------|----|----|----|------------------|
| $\overline{OE}$ | S2 | S1 | S0 |                  |
| L               | L  | L  | L  | A port = B1 port |
| L               | L  | L  | H  | A port = B2 port |
| L               | L  | H  | L  | A port = B3 port |
| L               | L  | H  | H  | A port = B4 port |
| L               | H  | L  | L  | A port = B5 port |
| L               | H  | L  | H  | A port = B6 port |
| L               | H  | H  | L  | A port = B7 port |
| L               | H  | H  | H  | A port = B8 port |
| H               | X  | X  | X  | Disconnect       |

logic diagram (positive logic)

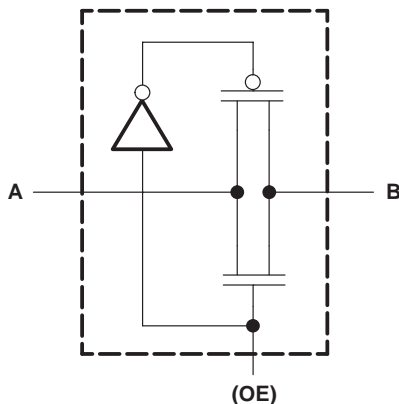


# SN74CBTLV3251

## LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS054I – MARCH 1998 – REVISED OCTOBER 2003

simplified schematic, each FET switch



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                 |
|--|-----------------|
| Supply voltage range, $V_{CC}$ .....                                   | -0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1) .....                          | -0.5 V to 4.6 V |
| Continuous channel current .....                                       | 128 mA          |
| Input clamp current, $I_K$ ( $V_{I/O} < 0$ ) .....                     | -50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... | 73°C/W          |
| (see Note 2): DBQ package .....  | 90°C/W          |
| (see Note 2): DGV package .....  | 120°C/W         |
| (see Note 2): PW package .....   | 108°C/W         |
| (see Note 3): RGY package .....  | 39°C/W          |
| Storage temperature range, $T_{Stg}$ .....                             | -65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 4)

|          |                                  | MIN  | MAX | UNIT |
|----------|----------------------------------|--|-----|------|
| $V_{CC}$ | Supply voltage                   | 2.3  | 3.6 | V    |
| $V_{IH}$ | High-level control input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | V    |
|          |                                  | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2   |      |
| $V_{IL}$ | Low-level control input voltage  | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 0.7 | V    |
|          |                                  | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 0.8 |      |
| $T_A$    | Operating free-air temperature   | -40  | 85  | °C   |

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74CBTLV3251

## LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS0541 – MARCH 1998 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                |   | TEST CONDITIONS             |   | MIN | TYP† | MAX      | UNIT          |
|--------------------------|---|-----------------------------|---|-----|------|----------|---------------|
| $V_{IK}$                 |   | $V_{CC} = 3\text{ V}$ ,     | $I_I = -18\text{ mA}$                                       |     |      | -1.2     | V             |
| $I_I$                    |   | $V_{CC} = 3.6\text{ V}$ ,   | $V_I = V_{CC}$ or GND                                       |     |      | $\pm 1$  | $\mu\text{A}$ |
| $I_{off}$                |   | $V_{CC} = 0$ ,              | $V_I$ or $V_O = 0$ to $3.6\text{ V}$                        |     |      | 20       | $\mu\text{A}$ |
| $I_{CC}$                 |   | $V_{CC} = 3.6\text{ V}$ ,   | $I_O = 0$ , $V_I = V_{CC}$ or GND                           |     |      | 10       | $\mu\text{A}$ |
| $\Delta I_{CC}^\ddagger$ | Control inputs  | $V_{CC} = 3.6\text{ V}$ ,   | One input at $3\text{ V}$ , Other inputs at $V_{CC}$ or GND |     |      | 300      | $\mu\text{A}$ |
| $C_i$                    | Control inputs  | $V_I = 3\text{ V}$ or $0$   |   |     |      | 3        | pF            |
| $C_{io(OFF)}$            | A port  | $V_O = 3\text{ V}$ or $0$ , | $\overline{OE} = V_{CC}$                                    |     |      | 40.5     | pF            |
|                          | B port  |                             |   |     |      | 6        |               |
| $r_{on}^\S$              | $V_{CC} = 2.3\text{ V}$ ,<br>TYP at $V_{CC} = 2.5\text{ V}$ | $V_I = 0$                   | $I_I = 64\text{ mA}$  | 5   | 8    | $\Omega$ |               |
|                          |   |                             | $I_I = 24\text{ mA}$  | 5   | 8    |          |               |
|                          |   | $V_I = 1.7\text{ V}$ ,      | $I_I = 15\text{ mA}$  | 27  | 40   |          |               |
|                          | $V_{CC} = 3\text{ V}$                                       | $V_I = 0$                   | $I_I = 64\text{ mA}$  | 5   | 7    |          |               |
|                          |   |                             | $I_I = 24\text{ mA}$  | 5   | 7    |          |               |
|                          |   | $V_I = 2.4\text{ V}$ ,      | $I_I = 15\text{ mA}$  | 10  | 15   |          |               |

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)        | TO (OUTPUT) | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | UNIT |
|-----------|---------------------|-------------|--|-----|--|-----|------|
|           |                     |             | MIN                                      | MAX | MIN                                      | MAX |      |
| $t_{pd}$  | A or B <sup>¶</sup> | B or A      | 0.15                                     |     | 0.25                                     |     | ns   |
|           | S                   | A           | 1  | 6.1 | 1  | 5.3 |      |
| $t_{en}$  | S                   | B           | 1  | 4.1 | 1  | 3.6 | ns   |
| $t_{dis}$ | S                   | B           | 1  | 3.5 | 1  | 3.3 | ns   |
| $t_{en}$  | $\overline{OE}$     | A or B      | 1  | 5.2 | 1  | 4.5 | ns   |
| $t_{dis}$ | $\overline{OE}$     | A or B      | 1  | 6.7 | 1  | 7.2 | ns   |

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

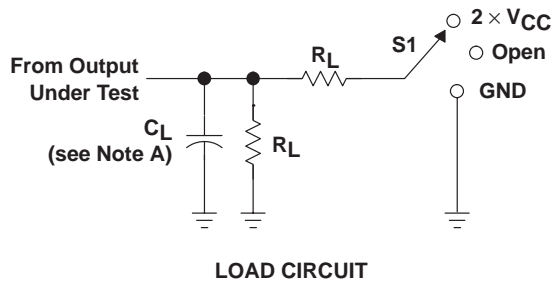


# SN74CBTLV3251

## LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

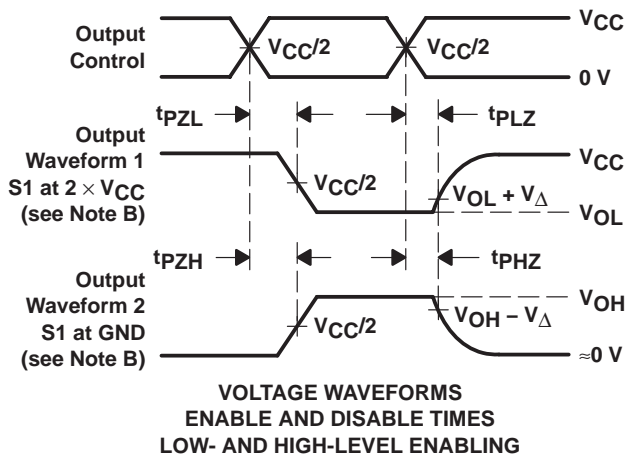
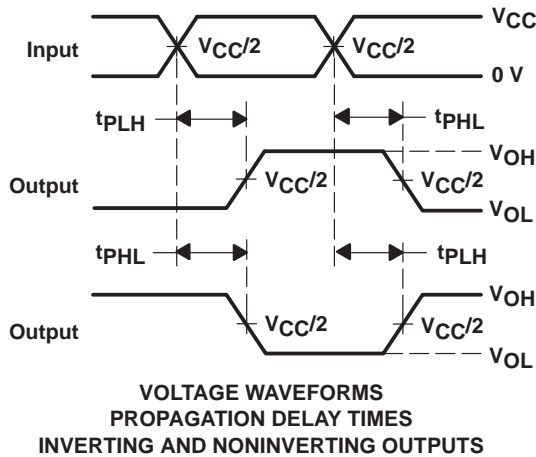
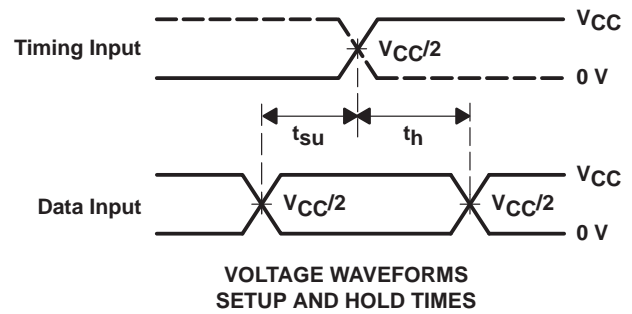
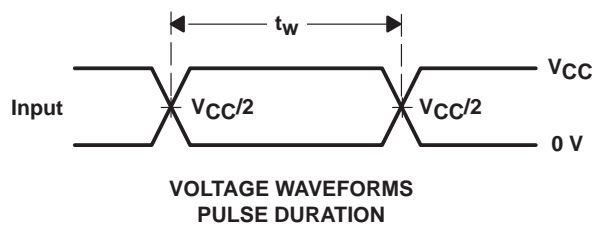
SCDS054I – MARCH 1998 – REVISED OCTOBER 2003

### PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

| $V_{CC}$          | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-------------------|-------|--------------|--------------|
| 2.5 V $\pm$ 0.2 V | 30 pF | 500 $\Omega$ | 0.15 V       |
| 3.3 V $\pm$ 0.3 V | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74CBTLV3251DBQRG4  | ACTIVE        | SSOP         | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | CL251                   | <a href="#">Samples</a> |
| SN74CBTLV3251D     | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3251               | <a href="#">Samples</a> |
| SN74CBTLV3251DBQR  | ACTIVE        | SSOP         | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | CL251                   | <a href="#">Samples</a> |
| SN74CBTLV3251DGVR  | ACTIVE        | TVSOP        | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CL251                   | <a href="#">Samples</a> |
| SN74CBTLV3251DR    | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3251               | <a href="#">Samples</a> |
| SN74CBTLV3251PWR   | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CL251                   | <a href="#">Samples</a> |
| SN74CBTLV3251RGRYR | ACTIVE        | VQFN         | RGY             | 16   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | CL251                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBTLV3251DBQR | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.5               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3251DGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3251DR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBTLV3251PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3251RGYR | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBTLV3251DBQR | SSOP         | DBQ             | 16   | 2500 | 340.5       | 338.1      | 20.6        |
| SN74CBTLV3251DGVR | TVSOP        | DGV             | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBTLV3251DR   | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74CBTLV3251PWR  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBTLV3251RGYR | VQFN         | RGY             | 16   | 3000 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

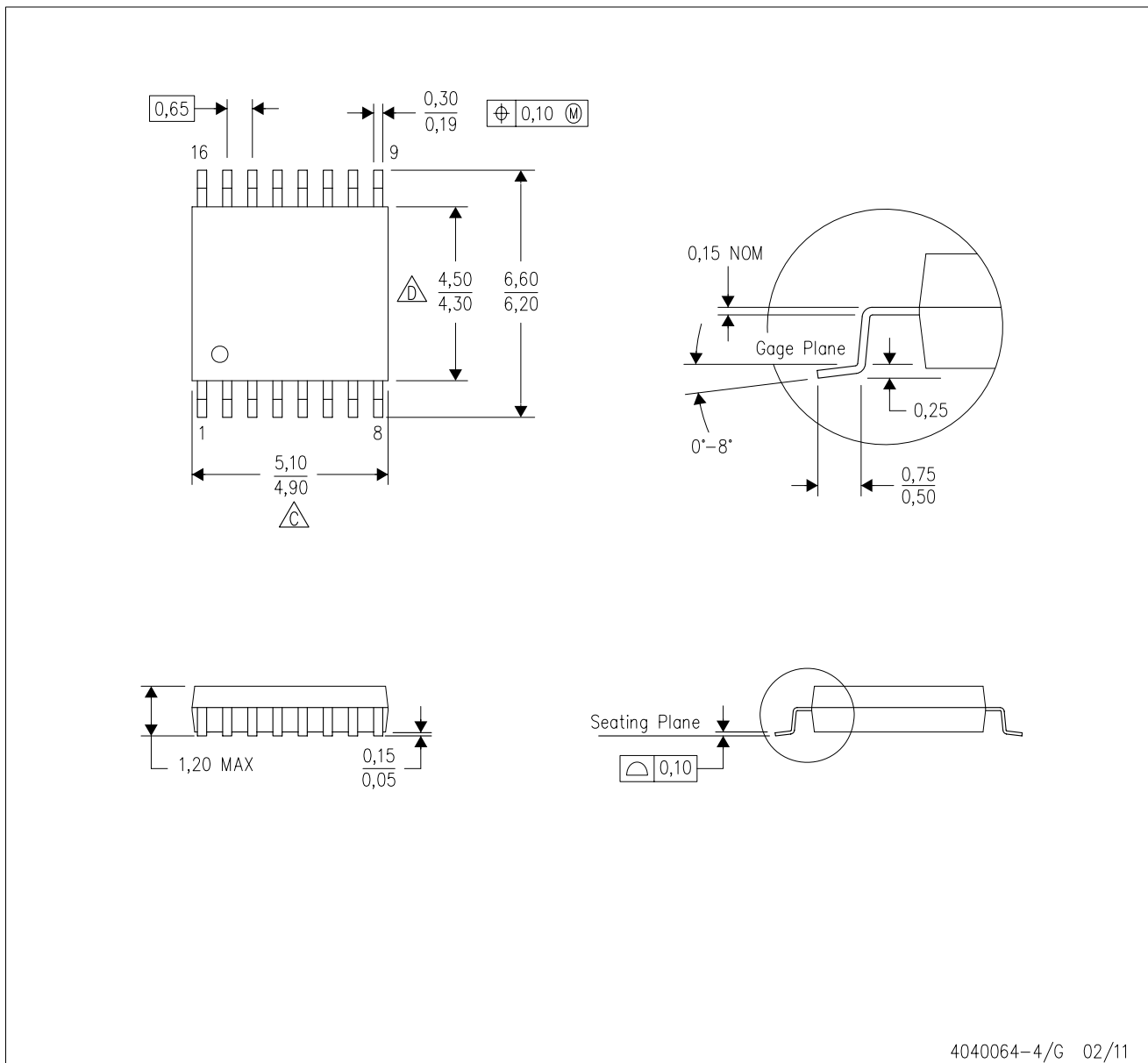
24 PINS SHOWN





- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

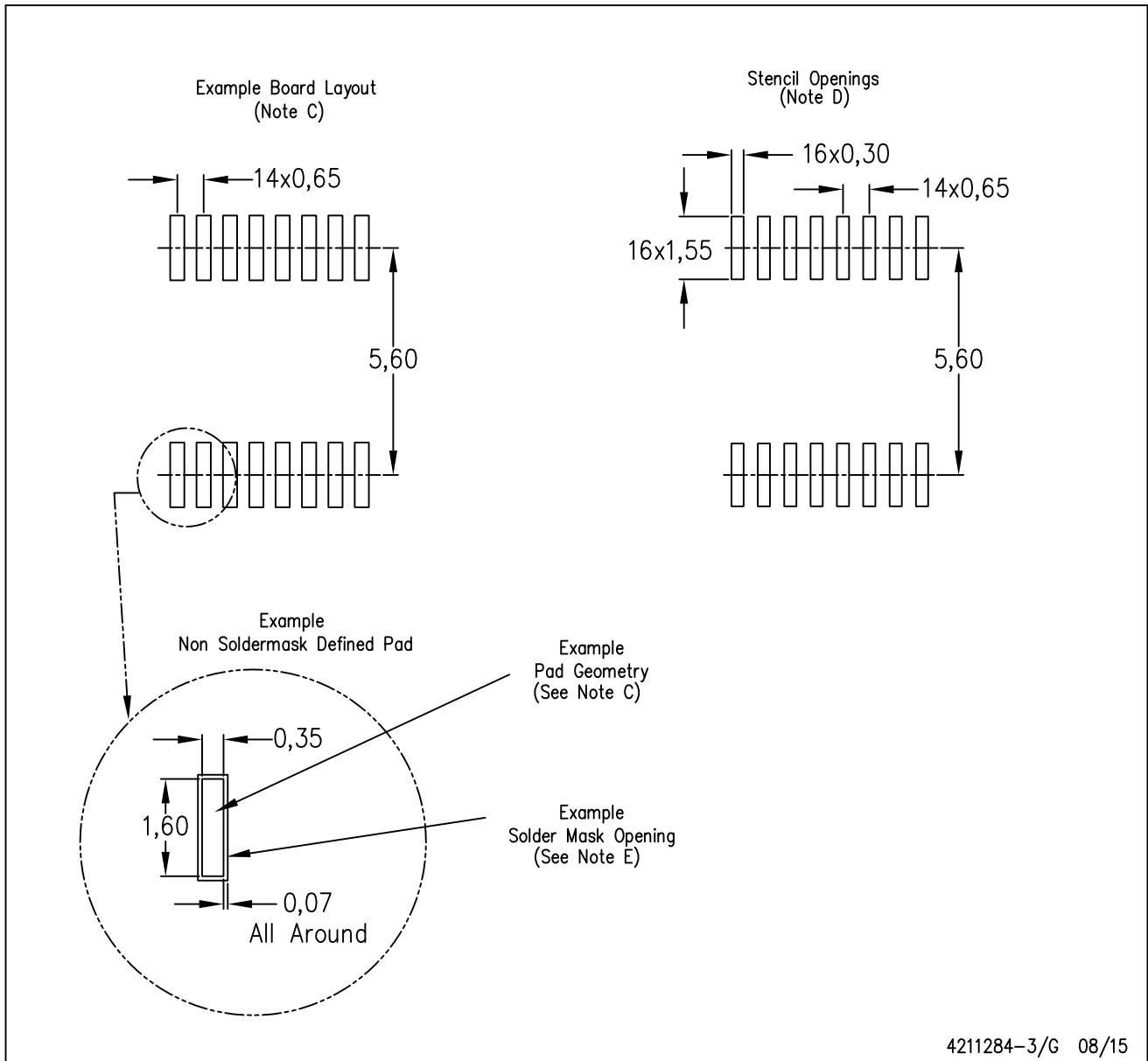


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/G 08/15

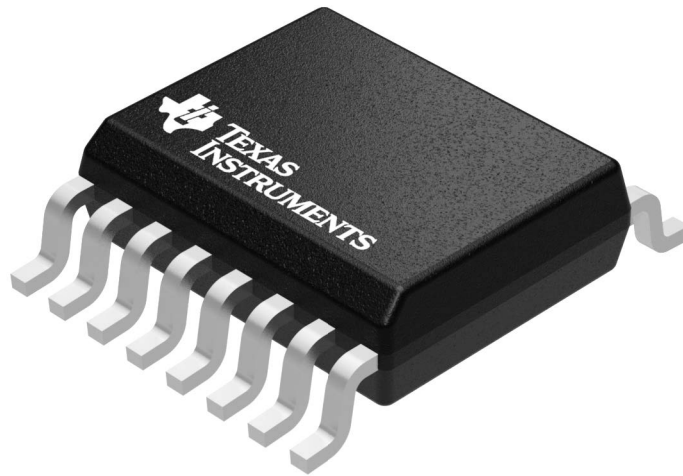
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**GENERIC PACKAGE VIEW**

**DBQ 16**

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073301-2/1



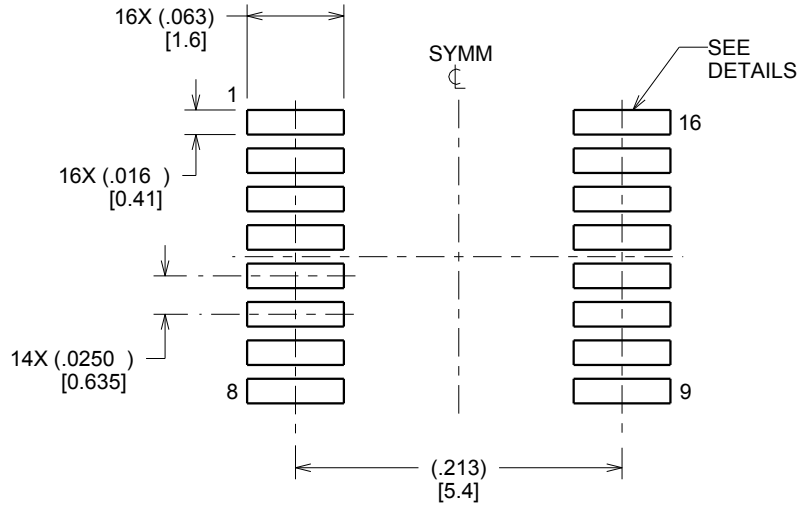


# EXAMPLE BOARD LAYOUT

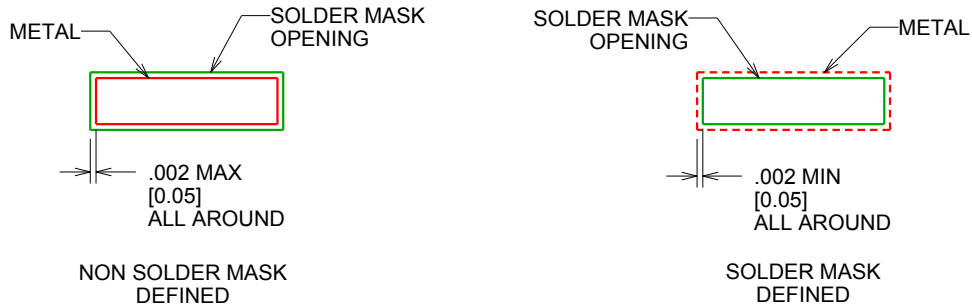
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

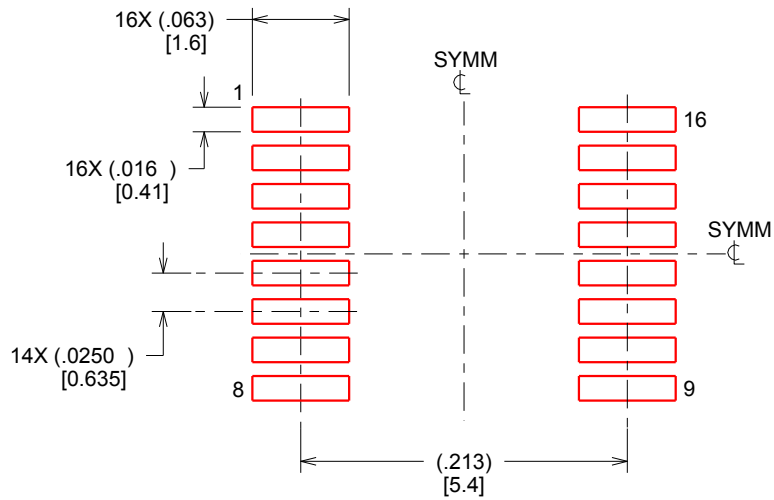
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

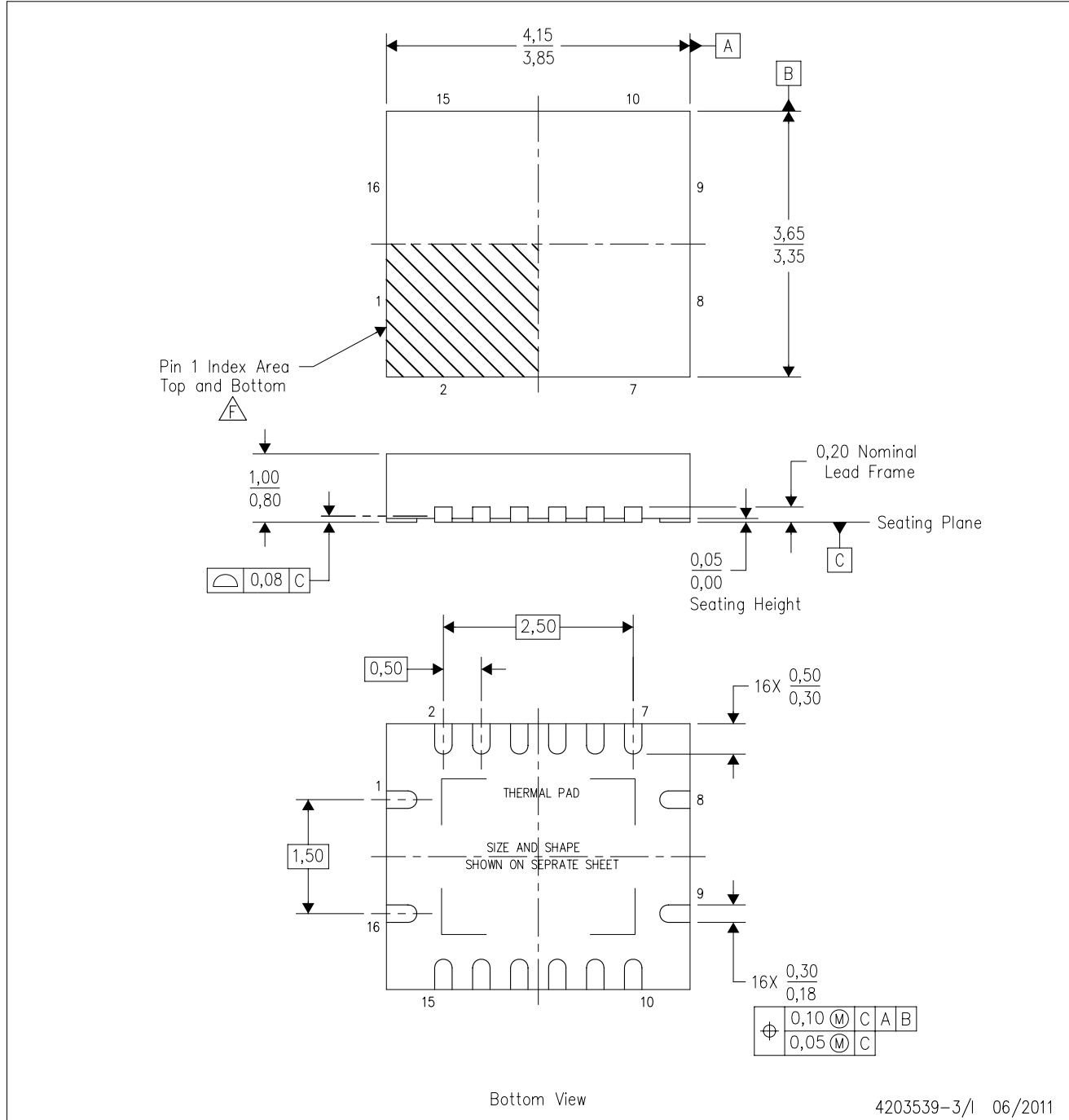
4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

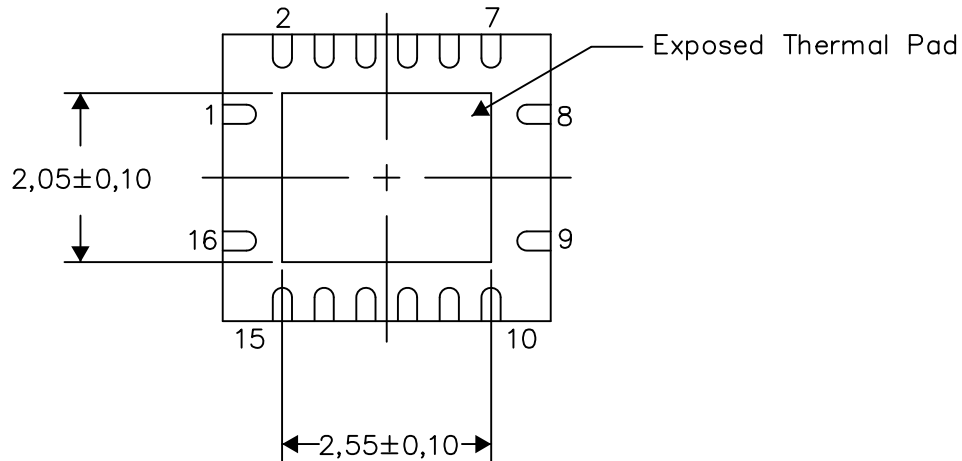
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

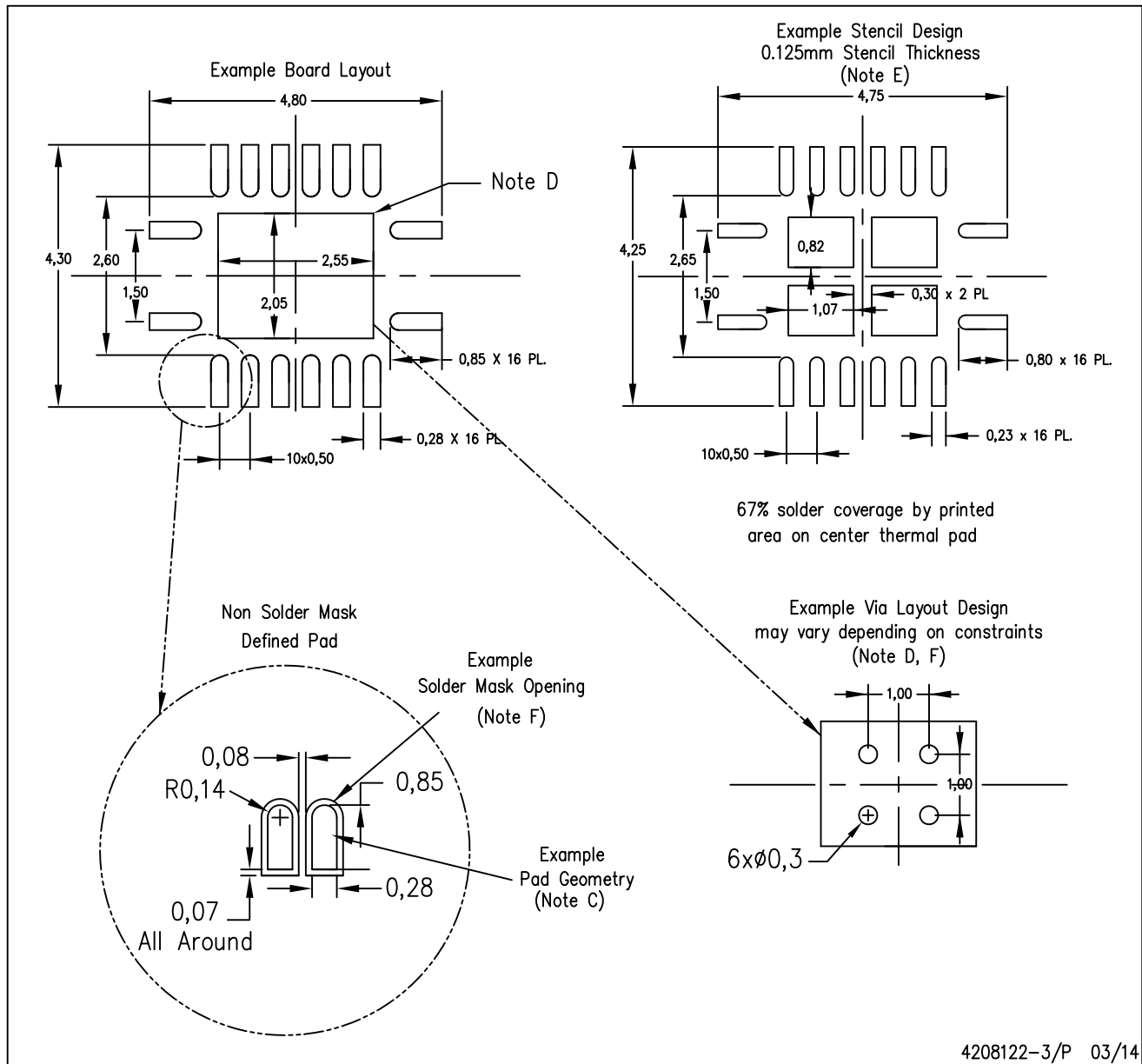
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2018, Texas Instruments Incorporated