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RF7321

3V LTE Band 11, 21 Linear PA Module

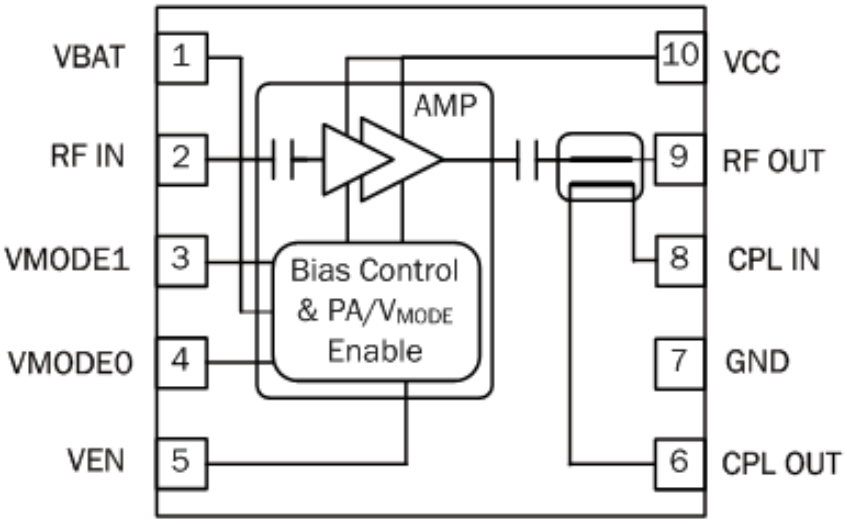
Package Style: Module, 10-Pin, 3mm x 3mm x 0.8mm

Features

- Fully Compliant to LTE Modulation
- LTE Bands 11, 21
- Best-in-Class Efficiency 47%, +28.5dBm Rel 99 output power
- High Power Gain : 28dB
- E-UTRA ACLR : -38dBc
- UTRA ACLR : -39dBc
- All LTE Channel Bandwidths (5 MHz up to 20 MHz)
- Optimized use with DC-DC converter Operation
- Three Power States with Digital Control Interface
- Integrated Power Coupler
- Integrated Blocking and Decoupling Capacitors

Applications

- LTE Handsets
- LTE Datacards



Functional Block Diagram

Product Description

The RF7321 is a high-power, high-efficiency linear power amplifier designed for use as final amplification stage in a 3V, 50 ohm LTE mobile cellular equipment. This PA is developed for the E-UTRAN\LTE Bands 11 and 21 for which operates in the 1427.9MHz to 1462.9MHz frequency band. The PA is specifically developed for 5MHz to 20MHz channel bandwidths used for the Band 11 or 21 operation on the LTE network. The RF7321 has two digital control pins to select one of three power bias states to optimize performance and current drain at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7321 is fully LTE compliant and is assembled in a 10-pin, 3mm x 3mm module.

Ordering Information

RF7321	3V LTE Band 11, 21 Linear PA Module
RF7321PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode	6.0	V
Supply Voltage, V_{BAT}	6.0	V
Control Voltage: V_{MODE0}, V_{MODE1}	3.5	V
Control Voltage: V_{EN}	3.5	V
RF - Input Power	+10	dBm
RF - Output Power	+30	dBm
Output Load VSWR (Ruggedness)	10:1	
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

P_{OUT} = 28. dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Operating Frequency Range	1427.9		1462.9	MHz	
V_{BAT}	+3.0	+3.8	+4.4	V	
V_{CC}	+0.5[1]	+3.4	+4.35	V	
V_{EN}, low level	0		0.5	V	PA disabled
V_{EN}, High level	1.5	1.8	3.1	V	PA enabled
V_{MODE0}, V_{MODE1}, low level	0		0.5	V	For a logic "low"
V_{MODE0}, V_{MODE1}, high level	1.5	1.8	3.1	V	For a logic "high"
Output Power (P_{OUT})					
Rel 99 Maximum Linear Output (HP)	+28.5[2]			dBm	High Power Mode (HP)
Rel 99 Maximum Linear Output (MP)	+17[2]			dBm	Medium Power Mode (MP)
Rel 99 Maximum Linear Output (LP)	+7[2]			dBm	Low Power Mode (LP)
LTE Maximum Linear Output (HP)	+27.5[2]			dBm	High Power Mode (HP), MPR=0
LTE Maximum Linear Output (MP)	+16[2]			dBm	Medium Power Mode (MP), MPR=0
LTE Maximum Linear Output (LP)	+6[2]			dBm	Low Power Mode (LP), MPR=0
Ambient Temperature	-30	25	+85	°C	

Notes:
[1] V_{CC} down to 0.5V may be used for backed-off power when using DC-DC converter to reduce low power current drain.
[2] For operation at V_{CC}=3.0V, de-rate P_{OUT} by 1.0dB and at V_{CC}=3.2V de-rate P_{OUT} by 0.5dB

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					Temp = +25C, V_{BAT}= +3.8V, V_{EN} = +1.8V, 50Ω system, LTE Modulation used: QPSK, 10MHz channel, 12 Resource Blocks with MPR = 0, unless otherwise specified.
Gain	26.5	28	31.5	dB	HP, P_{OUT} = 27.5dBm, V_{CC} = 3.4V
	17	19.5	23	dB	MP, $P_{OUT} \leq$ 16dBm, V_{CC} = 1.3V
	11	14	17	dB	LP, $P_{OUT} \leq$ 6dBm, V_{CC} = 0.7V
Gain Flatness		±0.25		dB	All modes over any 13.5MHz BW
Gain Linearity		±1		dB	All modes
ACLR - E-UTRA (±10MHz)		-39	-35	dBc	HP, P_{OUT} = 27.5dBm, V_{CC} = 3.4V (MPR=0)
		-39	-35	dBc	HP, P_{OUT} = 26.5dBm, V_{CC} = 3.4V[1]
		-41	-35	dBc	MP, $P_{OUT} \leq$ 16dBm, V_{CC} = 1.3V
		-44	-35	dBc	LP, $P_{OUT} \leq$ 6dBm, V_{CC} = 0.7V
ACLR1 - UTRA (±7.5MHz)		-39	-36	dBc	HP, P_{OUT} = 27.5dBm, V_{CC} = 3.4V (MPR=0)
		-39	-36	dBc	HP, P_{OUT} = 26.5dBm, V_{CC} = 3.4V[1]
		-41	-36	dBc	MP, $P_{OUT} \leq$ 16dBm, V_{CC} = 1.3V
		-44	-36	dBc	LP, $P_{OUT} \leq$ 6dBm, V_{CC} = 0.7V
ACLR2 - UTRA (±12.5MHz)		-62	-49	dBc	HP, P_{OUT} = 27.5dBm, V_{CC} = 3.4V (MPR=0)
		-42	-39	dBc	HP, P_{OUT} = 26.5dBm, V_{CC} = 3.4V[1]
		-62	-49	dBc	MP, $P_{OUT} \leq$ 16dBm, V_{CC} = 1.3V
		-62	-49	dBc	LP, $P_{OUT} \leq$ 6 dBm, V_{CC} = 0.7V
PA Efficiency (PAE)	39	43		%	HP, P_{OUT} = 27.5 dBm, V_{CC} = 3.4V
	35	40		%	HP, P_{OUT} = 26.5dBm, V_{CC} = 3.4V[1]
	25	29		%	MP, P_{OUT} = 16 dBm, V_{CC} = 1.3V
	10	12		%	LP, P_{OUT} = 6 dBm, V_{CC} = 0.7V
PA Current Drain		375	404	mA	HP, P_{OUT} = 27.5 dBm, V_{CC} = 3.4V
		320	375	mA	HP, P_{OUT} = 26.5dBm, V_{CC} = 3.4V[1]
		105	126	mA	MP, P_{OUT} = 16 dBm, V_{CC} = 1.3V
		39	46	mA	LP, P_{OUT} = 6 dBm, V_{CC} = 0.7V
PA + DC-DC Current Drain (MP)		42.3		mA	P_{OUT} = 16dBm, Assumes V_{BAT} = 3.8V, 85% DC-DC
PA + DC-DC Current Drain (LP)		9.6		mA	P_{OUT} = 6dBm, Assumes V_{BAT} = 3.8V, 75% DC-DC
Quiescent Current (PA only)		53	70	mA	HP, DC only, No RF applied
		37	50	mA	MP, DC only, No RF applied
		23	28	mA	LP, DC only, No RF applied
Quiescent Current (PA + DC-DC)		5.0		mA	No RF, with V_{CC}= 0.6V, V_{BAT} = 3.8V, and DC-DC Efficiency = 73%.
Noise Power in Duplex Rx Band 11		-135		dBm/Hz	All power outs, then measured at Rx Duplex Band 11 (Rx = 1476.9MHz to 1495.9MHz)
Noise Power in Duplex Rx Band 21		-135		dBm/Hz	All power outs, then measured at Rx Duplex Band 21 (Rx = 1495.9MHz to 1510.9MHz)
Noise Power in GPS Rx Band		-135		dBm/Hz	GPS Band RX at 1575.42MHz ± 1MHz
Noise Power in Band 1		-140		dBm/Hz	Measured in the 2110 - 2170 MHz band

NOTES:
[1] ACLR measurements were performed using 10MHz, QPSK LTE modulation with 50 resource blocks (MPR = 1dB) (reference 3GPP TS36.101)

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications (continued)					Temp = +25C, V_{BAT}= +3.8V, V_{EN} = +1.8V, 50Ω system, LTE Modulation used: QPSK, 10MHz channel, 12 Resource Blocks with MPR = 0, unless otherwise specified.
Noise Power in 2.4 GHz ISM Band		-143		dBm/Hz	Measured in the 2400 - 2483 MHz band
Noise Power in 5 GHz ISM Band		-146		dBm/Hz	Measured in the 4.9MHz to 5.9MHz band, excludes 3rd harmonic contributions
EVM		2.5	5	%	P_{OUT} ≤ +27.5 dBm, all power outs
Intermodulation (Channel BW offset)			-35	dBc	CW interferer at -42dBc at Channel BW Offset from carrier, P_{OUT} ≤ 27.5dBm
Intermodulation (2x Channel BW offset)			-41	dBc	CW interferer at -42dBc at (2 x Channel BW) Offset from carrier, P_{OUT} ≤ 27.5dBm
Input VSWR			1.8:1	VSWR	All modes
Spurious Output Levels			-70	dBc	All spurious, P_{OUT} ≤ 27.5dBm, all conditions, load VSWR at 6:1, all phase angles
Insertion Phase Shift		±25		°	Phase shift at +16dBm when switching from HP to MP, and then from MP to LP at +6dBm
Insertion Phase Shift Variation		±10		°	Part to part
DC Enable time			10	µS	Applied DC only, Time from V_{EN} = HIGH to stable idle current (90% of steady state value)
RF Rise time / RF Fall time			2	µS	
Coupling Factor		20		dB	P_{OUT} ≤ +27.5 dBm, all power outs
Coupling Accuracy - Temp/Voltage		±0.5		dB	P_{OUT} ≤ 27.5 dBm, all modes, -20°C ≤ T ≤ +85, V_{CC} as required , referenced back to 25°C, 3.4V nominal condition
Coupling Accuracy - VSWR		±0.25		dB	P_{OUT} ≤ 27.5 dBm, all modes, load VSWR 2:1, ± 0.25dB accuracy corresponds to 20dB coupler directivity
Coupler Insertion Loss		0.25		dB	For the daisy-chain couplers (PA-to-PA): CPL IN to CPL OUT; 698MHz to 2620MHz
Rel 99					
UMTS ACLR1 (±5MHz)		-40		dBc	HP, P_{OUT} = 28.5 dBm, V_{CC} = 3.4V
		-40		dBc	MP, P_{OUT} ≤ 17dBm, V_{CC}= 1.3V
		-40		dBc	LP, P_{OUT} ≤ 7dBm, V_{CC}= 0.7V
UMTS ACLR2 (±10MHz)		-52		dBc	HP, P_{OUT} = 28.5dBm, V_{CC} = 3.4V
		-52		dBc	MP, P_{OUT} ≤ 17dBm, V_{CC}= 1.3V
		-52		dBc	LP, P_{OUT} ≤ 7dBm, V_{CC}= 0.7V
PA Efficiency (PAE)		47		%	HP, P_{OUT} = 28.5dBm, V_{CC} = 3.4V
		32		%	MP, P_{OUT} = 17dBm, V_{CC}= 1.3V
		17		%	LP, P_{OUT} = 7dBm, V_{CC}= 0.7V
PA Current Drain		443		mA	HP, P_{OUT} = 28.5dBm, V_{CC} = 3.4V
		120		mA	MP, P_{OUT} = 17dBm, V_{CC}= 1.3V
		40		mA	LP, P_{OUT} = 7dBm, V_{CC}= 0.7V
PA + DC-DC Current Drain (MP)		48		mA	P_{OUT} = 17dBm, Assumes V_{BAT} = 3.8V, 85% DC-DC
PA + DC-DC Current Drain (LP)		10		mA	P_{OUT} = 7dBm, Assumes V_{BAT} = 3.8V, 75% DC-DC
UMTS EVM		2		%	All modes
Harmonics, $2F_O$			-35	dBc	P_{OUT} = +28.5 dBm
Harmonics,$3F_O$			-42	dBc	P_{OUT} = +28.5 dBm

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Pin-Out Description

Pin	Function	Description
1	VBAT	Supply voltage for the bias circuitry.
2	RF IN	RF input internally matched to 50Ω and DC blocked.
3	VMODE1	Digital control input for power mode selection.
4	VMODE0	Digital control input for power mode selection.
5	VEN	Digital control input for PA enable and disable.
6	CPL OUT	Coupler output.
7	GND	This pin must be grounded.
8	CPL IN	Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler.
9	RF OUT	RF output internally matched to 50Ω and DC blocked.
10	VCC	Supply voltage for the first and second stage amplifiers which can be connected to the battery supply or output of the DC-DC converter.
Pkg Base	GND	Ground connection - this package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

Operating Logic Table

V_{EN}	V_{MODE0}	V_{MODE1}	V_{BAT}	V_{CC}	Conditions/Comments
Low	Low	Low	3.0V to 4.4V	0.5V to 4.35V	Power down mode
Low	X	X	3.0V to 4.4V	0.5V to 4.35V	Standby Mode
High	Low	Low	3.0V to 4.4V	0.5V to 4.35V	High Power State
High	High	Low	3.0V to 4.4V	0.5V to 4.35V	Medium Power State
High	High	High	3.0V to 4.4V	0.5V to 4.35V	Low Power State

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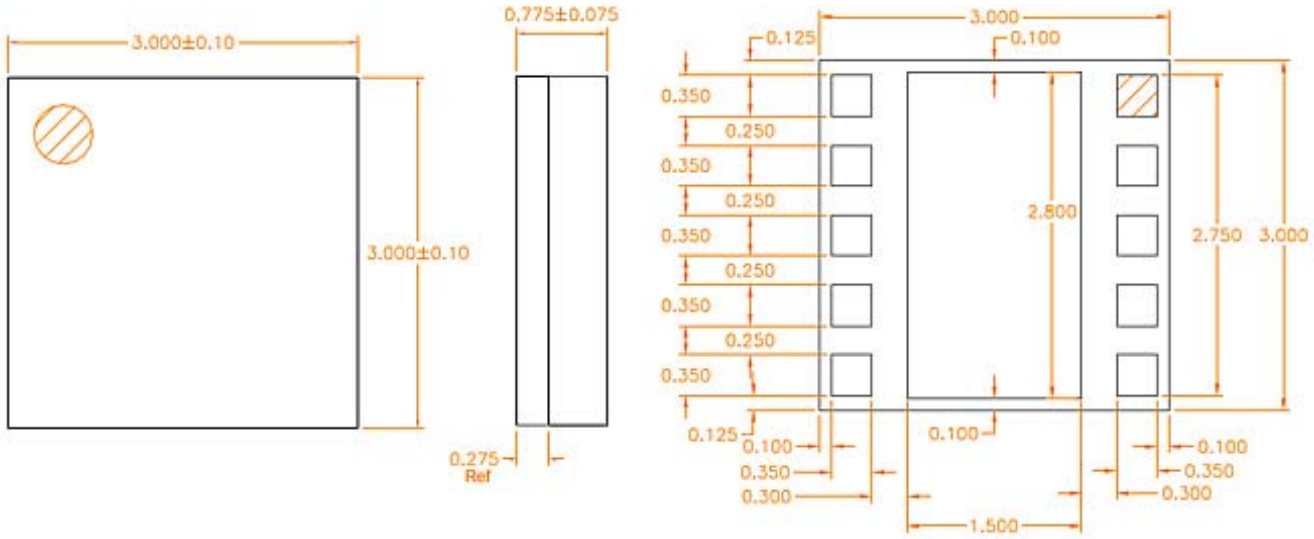
Package Drawing



Notes:
1. Shaded area represents Pin 1 location.

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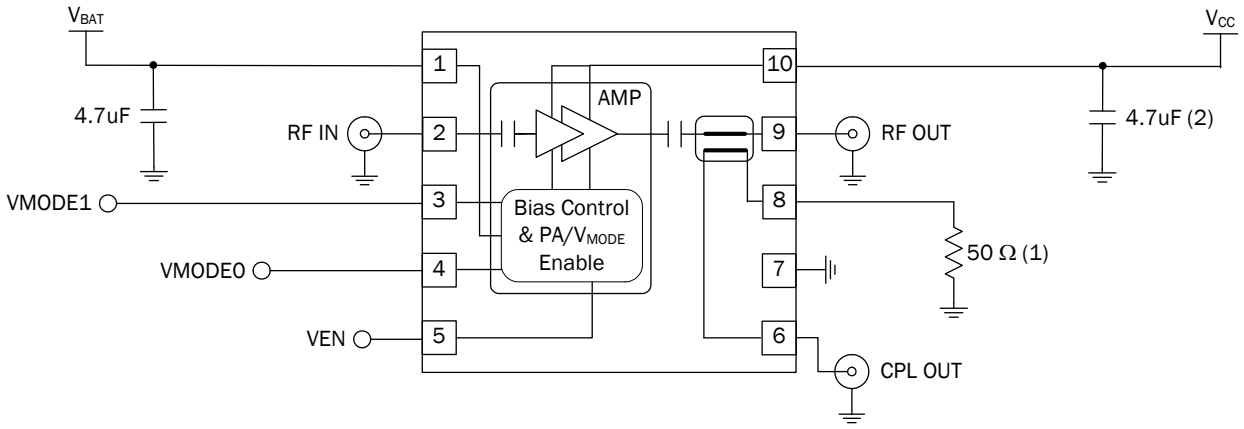
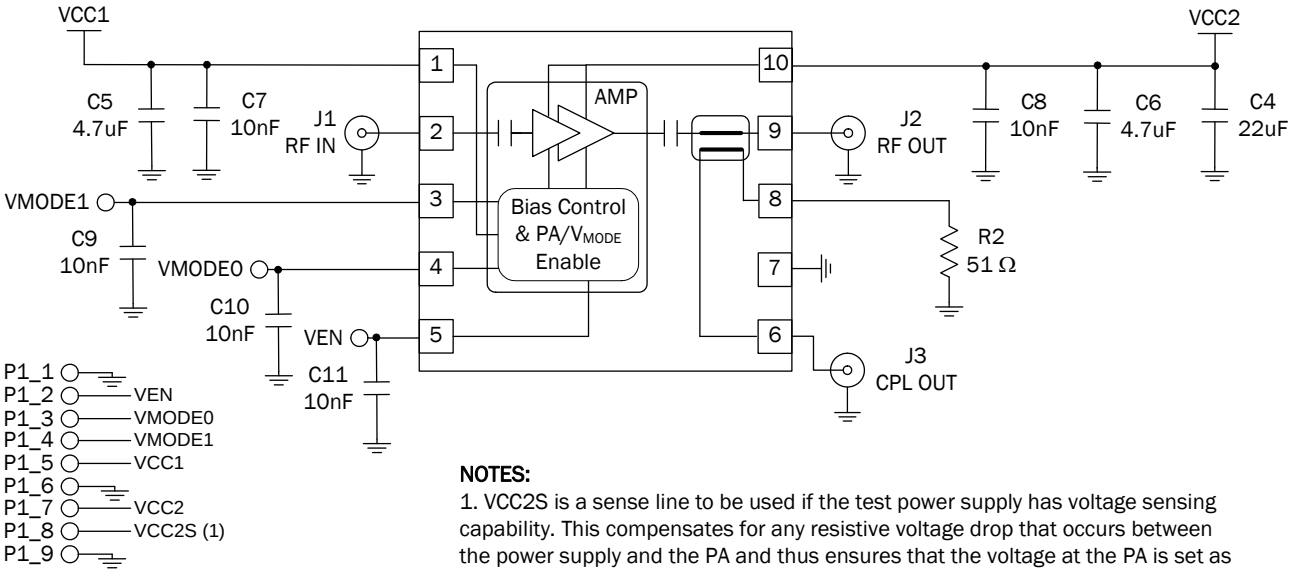
Preliminary Application Schematic



NOTES:

1. The 50Ω resistor should be removed if pin 8 is connected to another coupler for daisy chaining multiple couplers.
2. This capacitance value can be reduced for multi-PA with DC to DC converter applications where a total maximum capacitive load is required to be met. Keeping at least a 1uF capacitor close to the PA Vcc pin is recommended.

Evaluation Board Schematic



NOTES:

1. VCC2S is a sense line to be used if the test power supply has voltage sensing capability. This compensates for any resistive voltage drop that occurs between the power supply and the PA and thus ensures that the voltage at the PA is set as expected.

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PCB Design Requirements

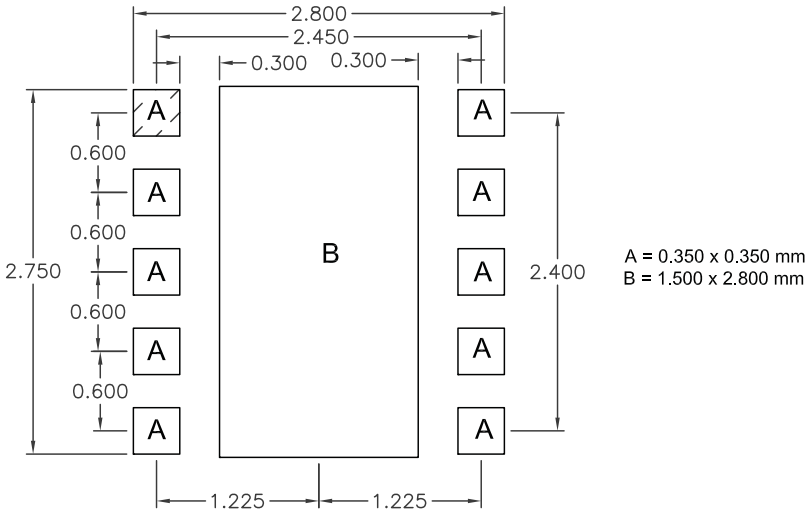
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern (Top View)



PCB METAL LAND PATTERN

Notes:
1. Shaded area represents Pin 1 location

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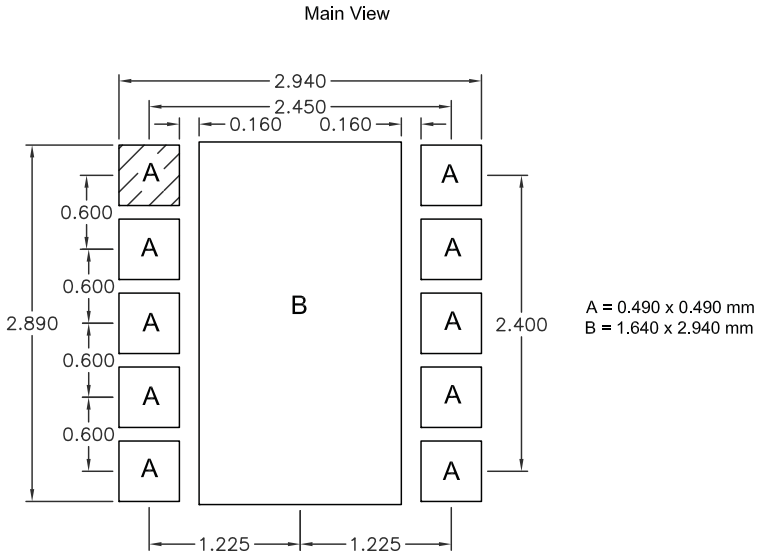
PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

PCB Solder Mask Pattern (Top View)



PCB SOLDER MASK PATTERN

Notes:
1. Shaded area represents Pin 1 location

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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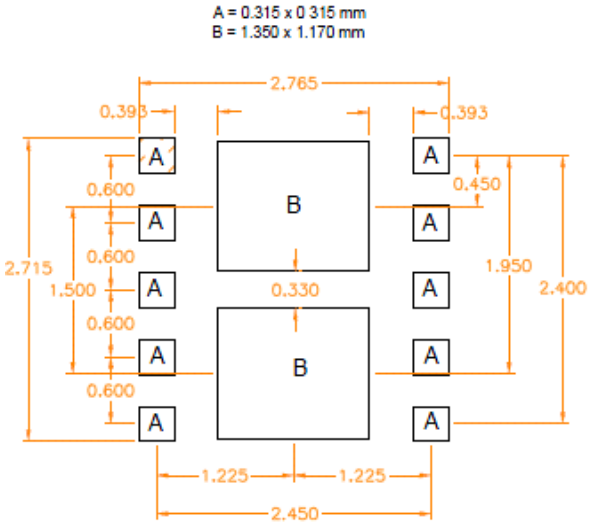
PCB Stencil Pattern (Top View)



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