MP1499

High Efficiency 5A Peak, 16V, 500kHz Synchronous Step Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1499 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 5A peak output current over a wide input supply range with excellent load and line regulation. The MP1499 has synchronous mode operation for higher efficiency over output current load range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include over current protection and thermal shut down.

The MP1499 requires a minimum number of readily available standard external components and is available in a space saving 10-pin QFN (2x3mm) package.

FEATURES

- Wide 4.5V to 16V Operating Input Range
- 70mΩ/25mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Fixed 500kHz Switching Frequency
- Sync from 200kHz to 2MHz External Clock
- AAM Power Save Mode
- External Soft Start
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN10 (2x3mm) Package

APPLICATIONS

- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Distributed Power Systems

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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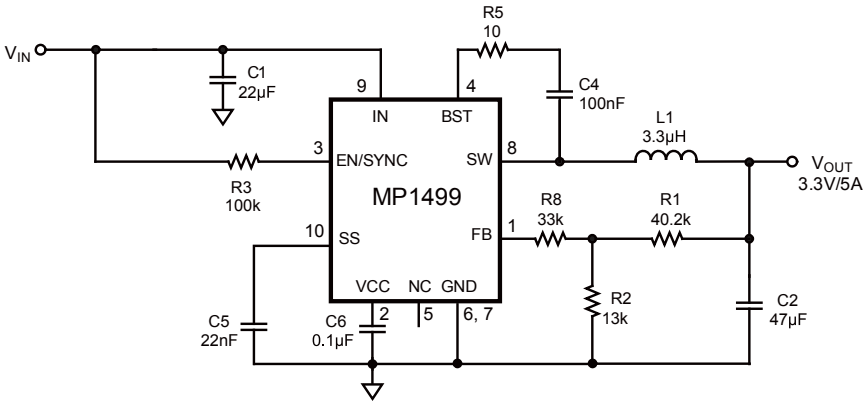
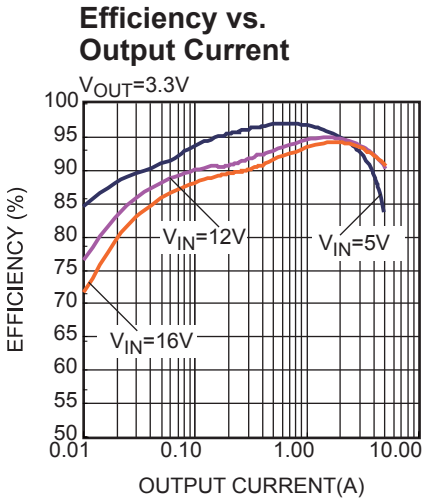
TYPICAL APPLICATION



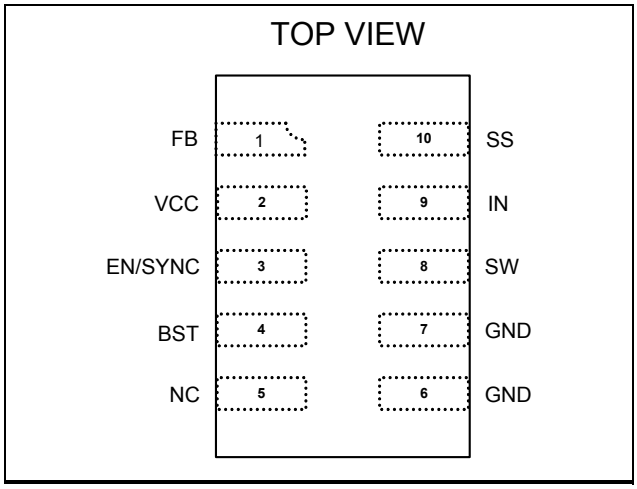


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1499GD	QFN10 (2x3mm)	ADH

* For Tape & Reel, add suffix –Z (e.g.MP1499GD–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....–0.3V to 17V
V_{SW} .....
-0.3V (-5V for <10ns) to 17V(19V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins.....–0.3V to 6.5 V(2)
Continuous Power Dissipation (T_A = +25°C) (3)
..... 1.92W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} .....4.5V to 16V
Output Voltage V_{OUT}..... 0.807V to VIN*D_{MAX}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN10 (2x3mm)	65	13 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to page 10, EN/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.6	1	mA
MOSFET						
HS Switch On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		70		mΩ
LS Switch On Resistance	LS_{RDS-ON}	V_{CC}=5V		25		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
MOSFET						
Current Limit (6)	I_{LIMIT}	40% Duty Cycle	7	9		A
Oscillator and Timer						
Oscillator Frequency	f_{SW}	V_{FB}=750mV	430	500	580	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV	90	95		%
Minimum On Time(6)	T_{ON_MIN}			60		ns
Sync Frequency Range	f_{SYNC}		0.2		2	MHz
Reference And Soft Start						
Feedback Voltage	V_{FB}	T_A=25°C	791	807	823	mV
		-40°C <T_A<85°C (7)	787	807	827	
Feedback Current	I_{FB}	V_{FB}=800mV		10	50	nA
Soft-Start Current	I_{SS}		8	11	14	μA
Enable And UVLO						
EN Rising Threshold	V_{EN_RISING}		1.2	1.4	1.6	V
EN Falling Threshold	$V_{EN\_FALLING}$		1.1	1.25	1.4	V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0		0		μA
EN Turn Off Delay	EN_{Td-off}			8		μs
VIN Under Voltage Lockout Threshold-Rising	$INUV_{Vth}$		3.7	3.9	4.1	V
VIN Under Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			650		mV
VCC Regulator						
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		3		%
Thermal Protection						
Thermal Shutdown(6)				150		ºC
Thermal Hysteresis(6)				20		ºC

Notes:

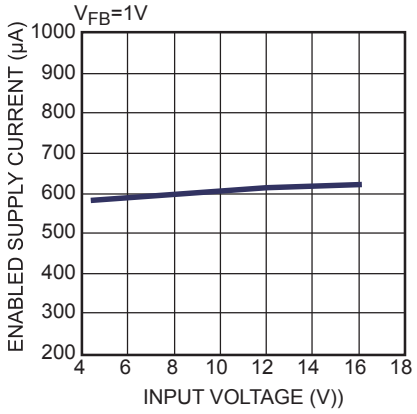
6) Guaranteed by design.

7) Not tested in production and guaranteed by over-temperature characterization.

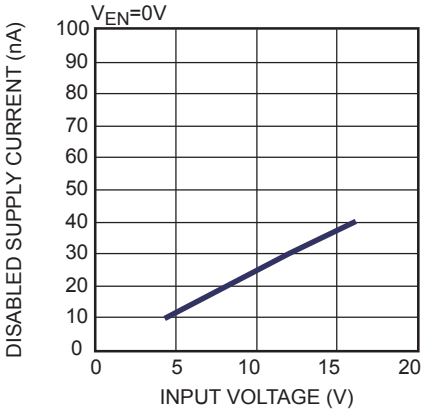
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

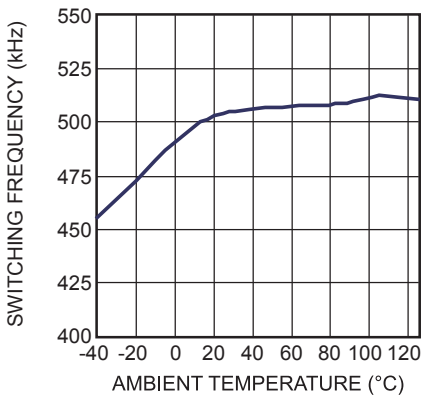
Enabled Supply Current vs. Input Voltage



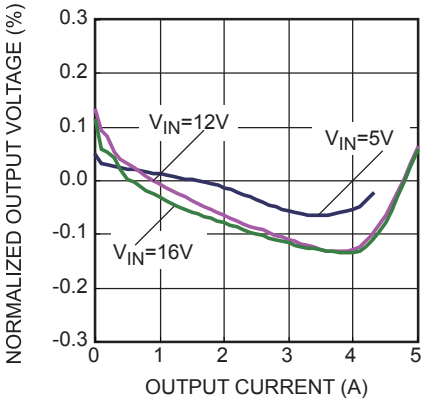
Disabled Supply Current vs. Input Voltage



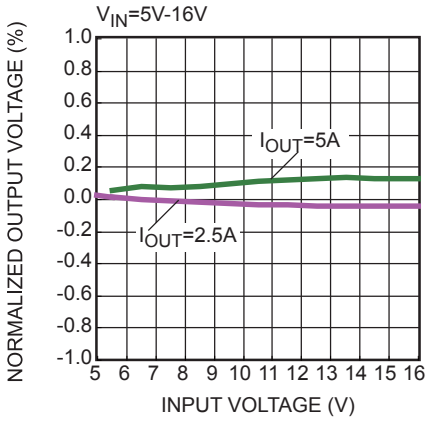
Switching Frequency vs. Ambient Temperature



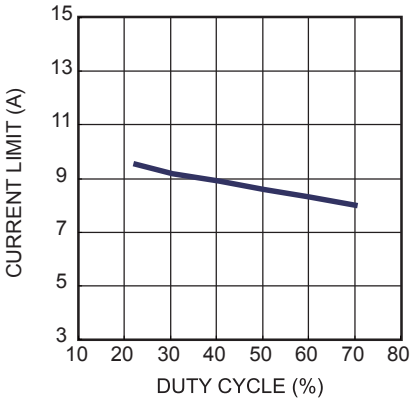
Load Regulation



Line Regulation



Current Limit vs. Duty Cycle

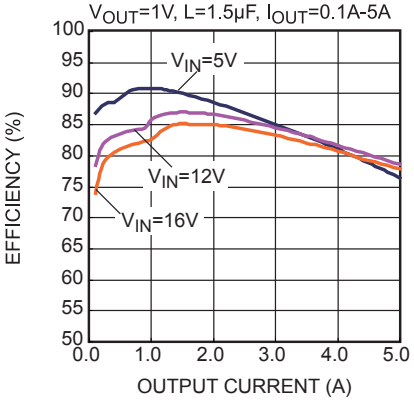


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

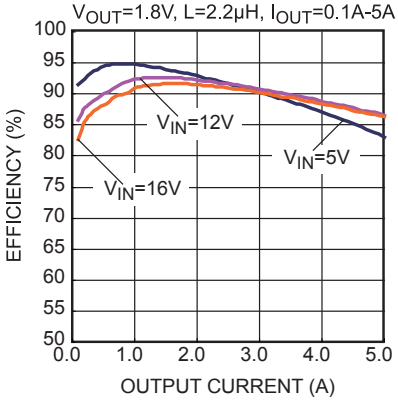
Efficiency vs. Output Current

V_{OUT}=1V, L=1.5µF, I_{OUT}=0.1A-5A



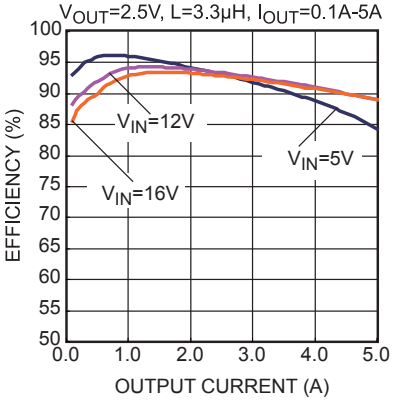
Efficiency vs. Output Current

V_{OUT}=1.8V, L=2.2µH, I_{OUT}=0.1A-5A



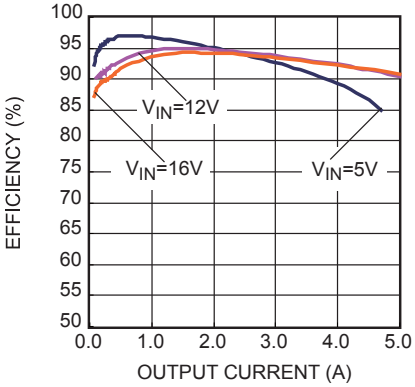
Efficiency vs. Output Current

V_{OUT}=2.5V, L=3.3µH, I_{OUT}=0.1A-5A



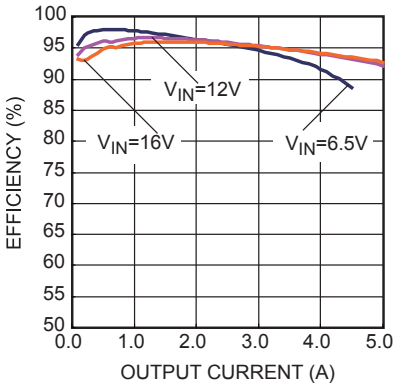
Efficiency vs. Output Current

V_{OUT}=3.3V, L=3.3µH, I_{OUT}=0.1A-5A



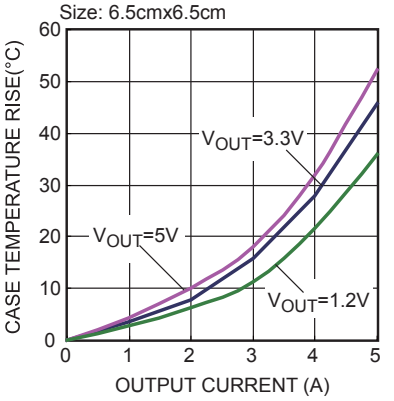
Efficiency vs. Output Current

V_{OUT}=5V, L=4.7µH, I_{OUT}=0.1A-5A



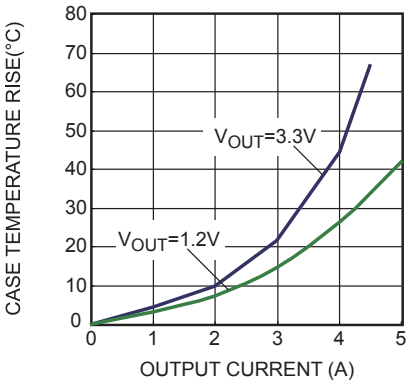
Case Temperature Rise vs. Output Current

V_{IN}=12V, I_{OUT}=0A-5A, 4 layers PCB, Size: 6.5cmx6.5cm



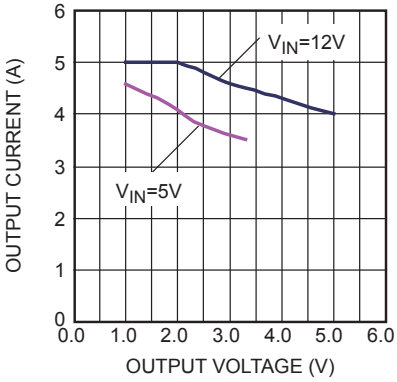
Case Temperature Rise vs. Output Current

V_{IN}=5V, I_{OUT}=0A-5A, 4 layers PCB, Size: 6.5cmx6.5cm



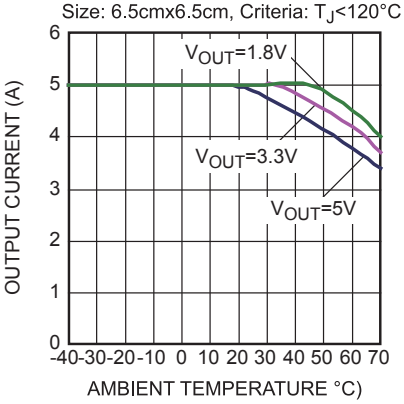
Output Current Derating vs. Output Voltage

2 layers PCB, Size: 6.5cmx6.5cm, Criteria: Trise<45°C



Output Current Derating vs. Ambient Temperature

V_{IN}=12V, 2 layers PCB, Size: 6.5cmx6.5cm, Criteria: T_J<120°C

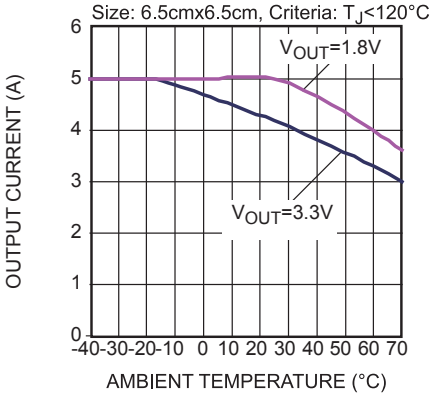


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

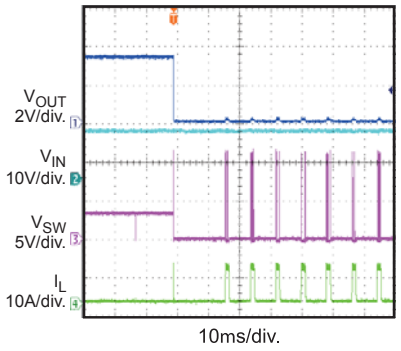
Output Current Derating vs. Ambient Temperature

V_{IN}=5V, 2 layers PCB,
Size: 6.5cmx6.5cm, Criteria: T_J<120°C



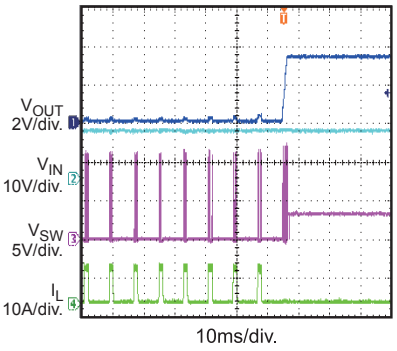
Short Entry

I_{OUT}=0A



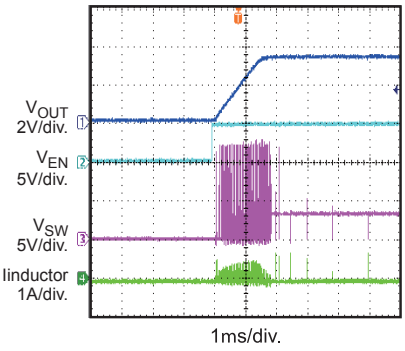
Short Recovery

I_{OUT}=0A



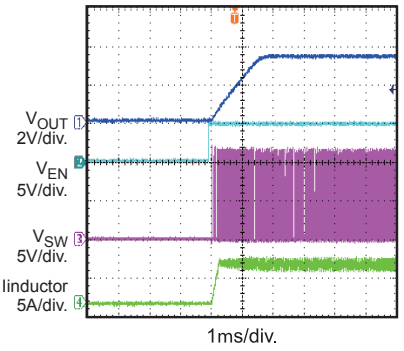
Startup through Enable

I_{OUT}=0A



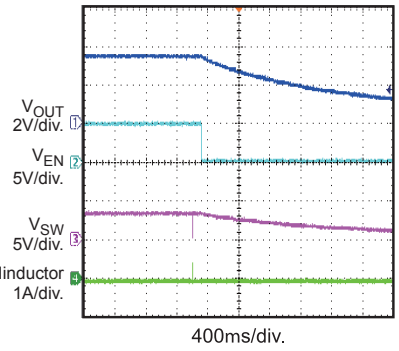
Startup through Enable

I_{OUT}=5A



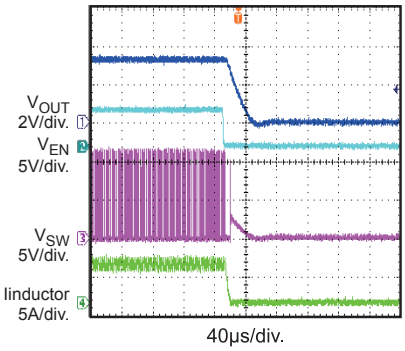
Shutdown through Enable

I_{OUT}=0A



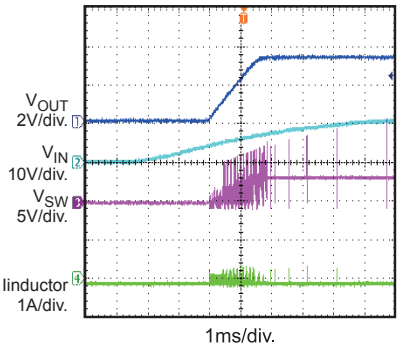
Shutdown through Enable

I_{OUT}=5A



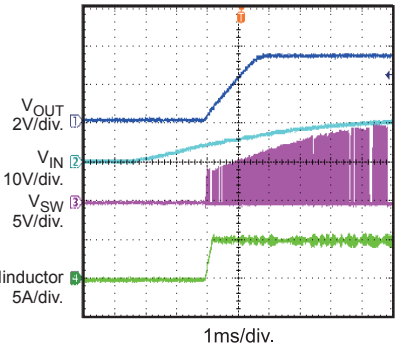
Startup through Input Voltage

I_{OUT}=0A



Startup through Input Voltage

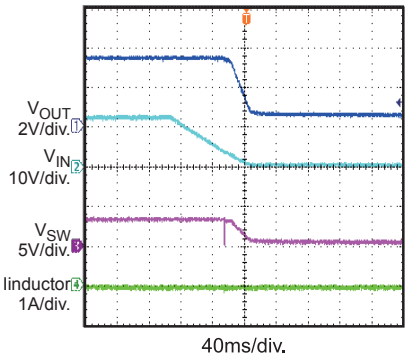
I_{OUT}=5A



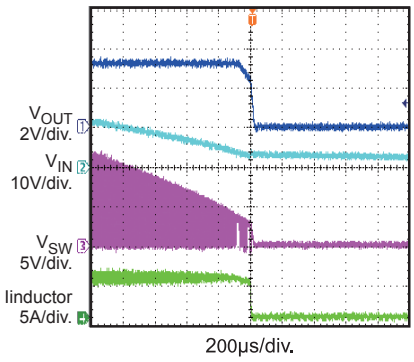
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

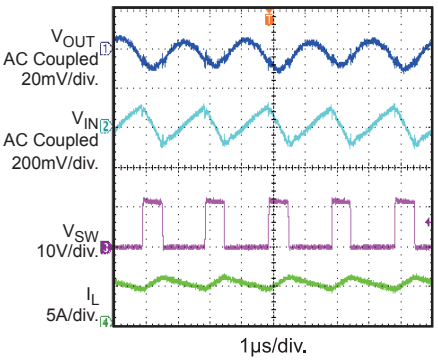
Shutdown through Input Voltage
I_{OUT}=0A



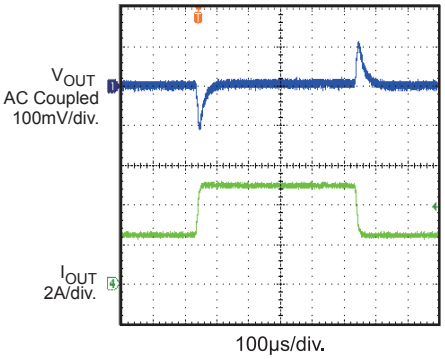
Shutdown through Input Voltage
I_{OUT}=5A



Input / Output Ripple
I_{OUT}=5A



Load Transient Reponse
I_{OUT}=2.5A-5A



PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV. It is recommended to place the resistor divider as close to FB pin as possible. Vias should be avoided on the FB traces.
2	VCC	Internal 5V LDO output. The driver and control circuits are powered from this voltage. Decouple with 0.1μF-0.22μF cap. And the capacitance should be no more than 0.22μF.
3	EN/SYNC	EN=high to enable the MP1499. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN with 100KΩ resistor.
4	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
5	NC	No connection internal. This pin can connect to GND.
6, 7	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Suggested to be connected to GND with copper and vias.
8	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the low-side switch and the internal body diode fixes the negative voltage. Use wide PCB traces and multiple vias to make the connection.
9	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP1499 operates from a +4.5V to +16V input rail. Low ESR, and low inductance capacitor C1 is needed to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias to make the connection.
10	SS	Soft Start. Connect on external capacitor to program the soft start time for the switch mode regulator.

FUNCTIONAL BLOCK DIAGRAM

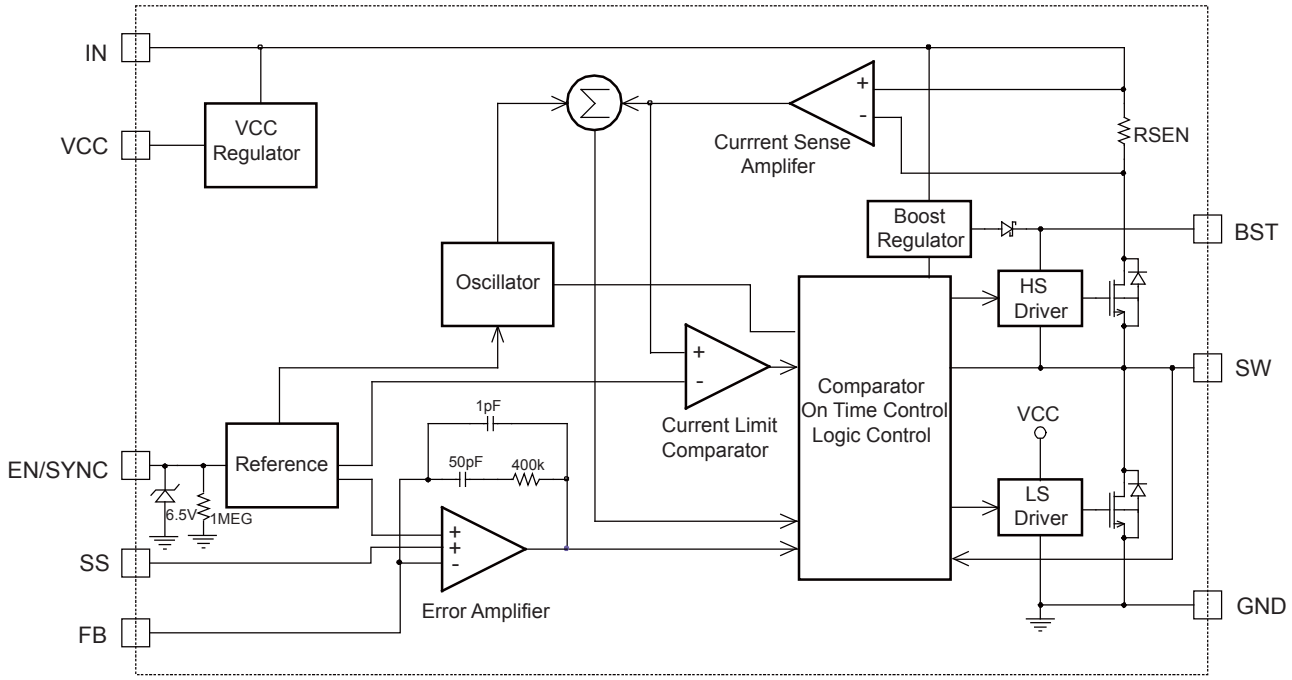


Figure 1—Functional Block Diagram

OPERATION

The MP1499 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 5A peak output current over a wide input supply range with excellent load and line regulation.

The MP1499 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, a 0.1uF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.807V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable/SYNC control

EN/Sync is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive it low to turn it off. There is an internal 1MΩ resistor from EN/Sync to GND thus EN/Sync can be floated to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 2. Connecting the EN input pin through a pullup resistor to the voltage on the V_{IN} pin limits the EN input current to less than 100μA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V – 6.5V) \div 100\mu A = 55k\Omega$.

Connecting the EN pin directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ⩽6V to prevent damage to the Zener diode.

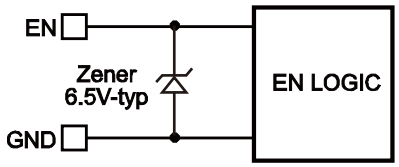


Figure 2—6.5V Zener Diode Connection

The chip can be synchronized to external clock range from 200kHz up to 2MHz through this pin as soon as an external clock is added to this pin, with the internal clock rising edge synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

The MP1499 has under-voltage lock-out protection (UVLO). When the VCC voltage is higher than the UVLO rising threshold voltage, the MP1499 will be powered up. It shuts off when the VCC voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

The MP1499 is disabled when the input voltage falls below 3.25 V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 3 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (VSTOP) above 4.5V. The rising threshold (VSTART) should be set to provide enough hysteresis to allow for any input supply variations.

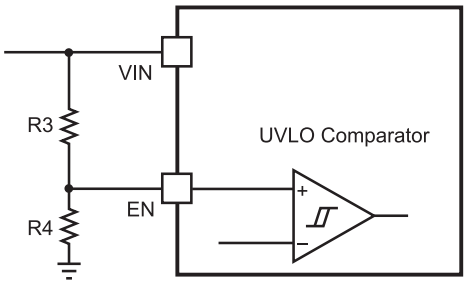


Figure 3—Adjustable UVLO

Soft-Start

The MP1499 employs soft start (SS) mechanism to ensure smooth output during power-up. When the EN pin becomes high, an internal current source (11μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

If the output is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

The SS capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. Otherwise, it's easy to hit the current limit during SS. A minimum value of 4.7nF should be used if the output capacitance value is larger than 330μF.

Power Save Mode for Light Load Condition

The MP1499 has AAM (Advanced Asynchronous Modulation) power save mode for light load. The AAM voltage is set at 0.4V internally. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} is higher than V_{AAM}.

Under the light load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}, during this time, the internal clock is blocked, thus the MP1499 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

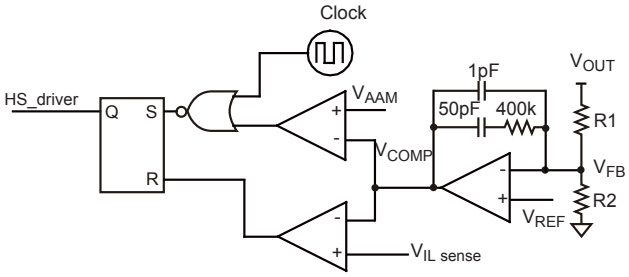


Figure 4—Simplified AAM Control Logic

When the load current is light, the inductor peak current is set internally which is about 1A for V_{IN}=12V, V_{OUT}=3.3V, and L=3.3μH.The curve of inductor peak current vs. inductor is shown in Figure 5.

Inductor Peak Current vs. Inductor

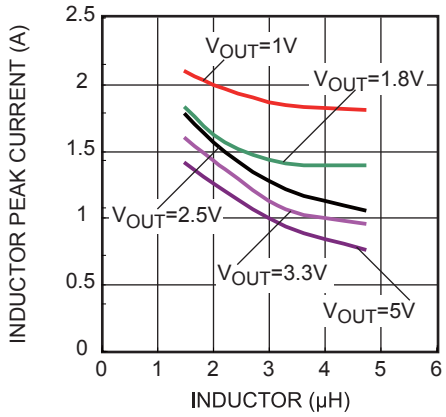


Figure5—Inductor Peak Current vs. Inductor

Over-Current-Protection and Hiccup

The MP1499 has cycle-by-cycle over current limit when the inductor current peak value

exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 50% below the reference. Once a UV is triggered, the MP1499 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP1499 exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (Figure 6). If (V_{IN}-V_{SW}) is more than 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4. A 10Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.

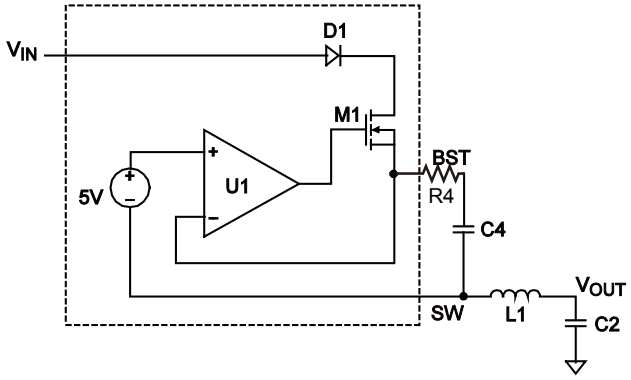


Figure 6—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 40kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1} \quad (2)$$

The T-type network is highly recommended when VOUT is low, as Figure 7 shows.

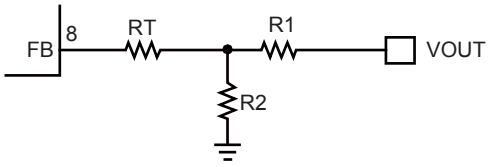


Figure 7— T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)
1	20.5(1%)	84.5(1%)	160(1%)
1.2	30.1(1%)	61.9(1%)	160(1%)
1.8	40.2(1%)	32.4(1%)	82(1%)
2.5	40.2(1%)	19.1(1%)	33(1%)
3.3	40.2(1%)	13(1%)	33(1%)
5	40.2(1%)	7.68(1%)	33(1%)

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, two pieces 22μF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worse case condition occurs at VIN = 2VOUT, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1499 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 8.

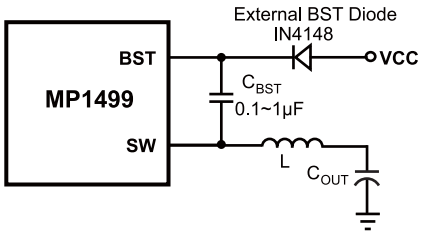


Figure 8—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1-1uF.

PC Board Layout [8]

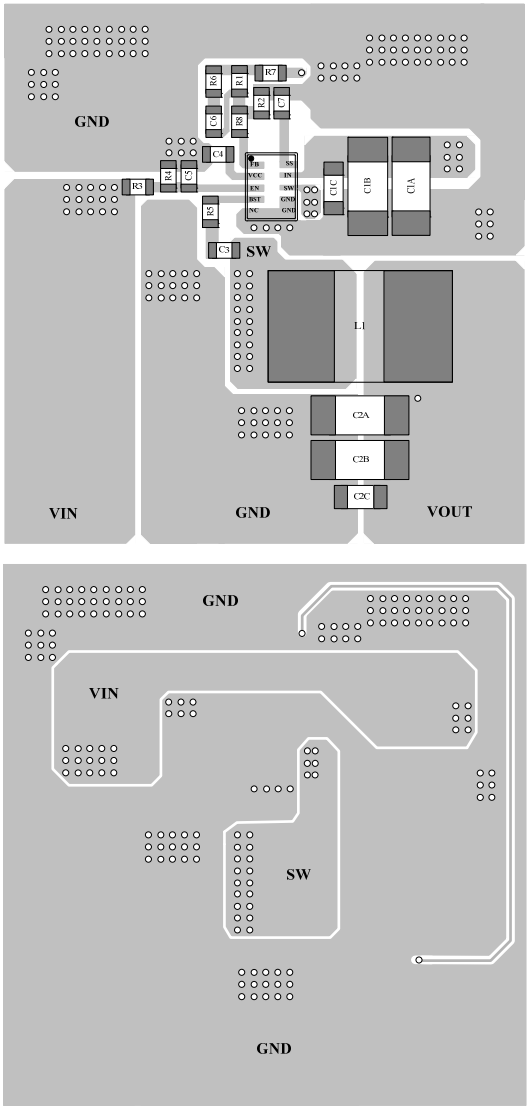
PCB layout is very important to achieve stable operation especially for VCC capacitor and input capacitor placement. For best results, follow these guidelines:

1) Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.
2) Place the VCC capacitor to VCC pin and GND pin as close as possible. Make the trace length of VCC pin-VCC capacitor anode-VCC capacitor cathode-chip GND pin as short as possible.
3) Place the ceramic input capacitor close to IN and GND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.

4) Route SW, BST away from sensitive analog areas such as FB. It's not recommended to route SW, BST trace under chip's bottom side.
5) Place the T-type feedback resistor R8 close to chip to ensure the trace which connects to FB pin as short as possible.

Notes:

8) The recommended layout is based on the Figure 9 Typical Application circuit on the next page.



Design Example

Below is a design example following the application guidelines for the specifications:

Table 2—Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	5A Peak

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

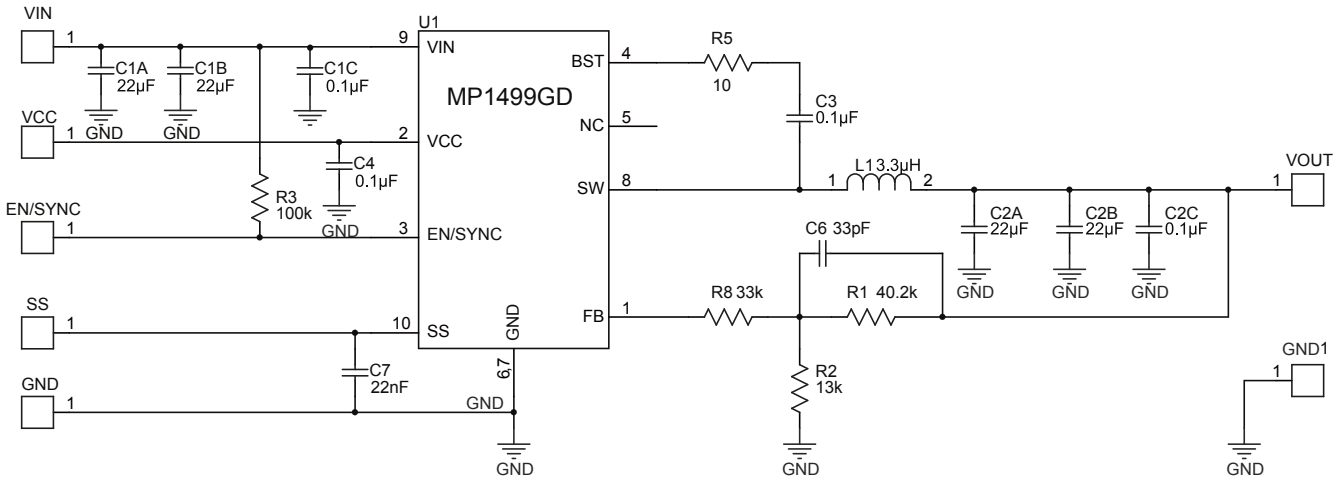


Figure 9—12V Input-3.3V/5A Peak Output

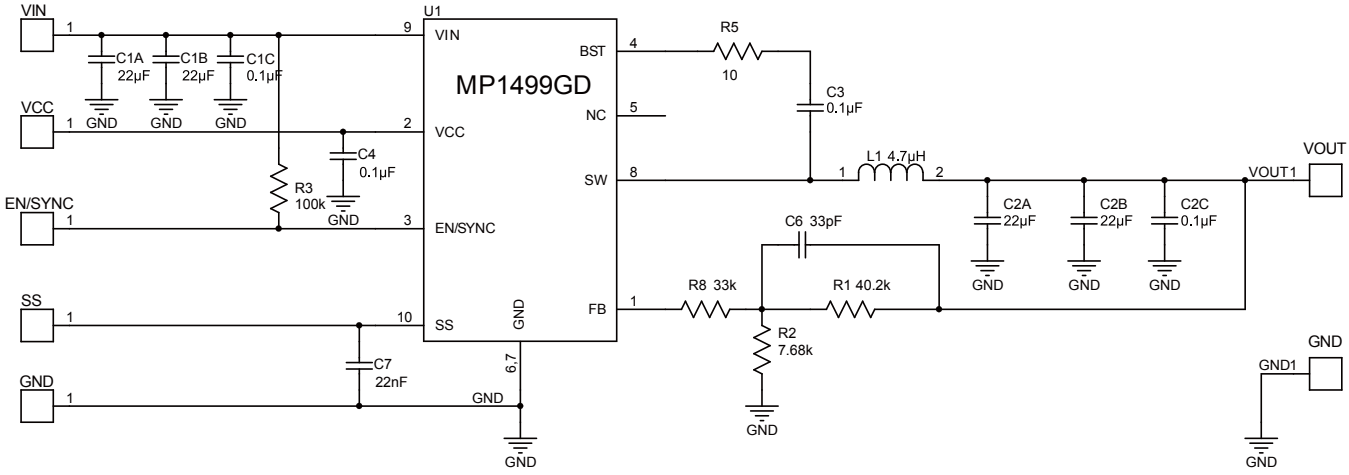


Figure 10—12V Input-5V/5A Peak Output

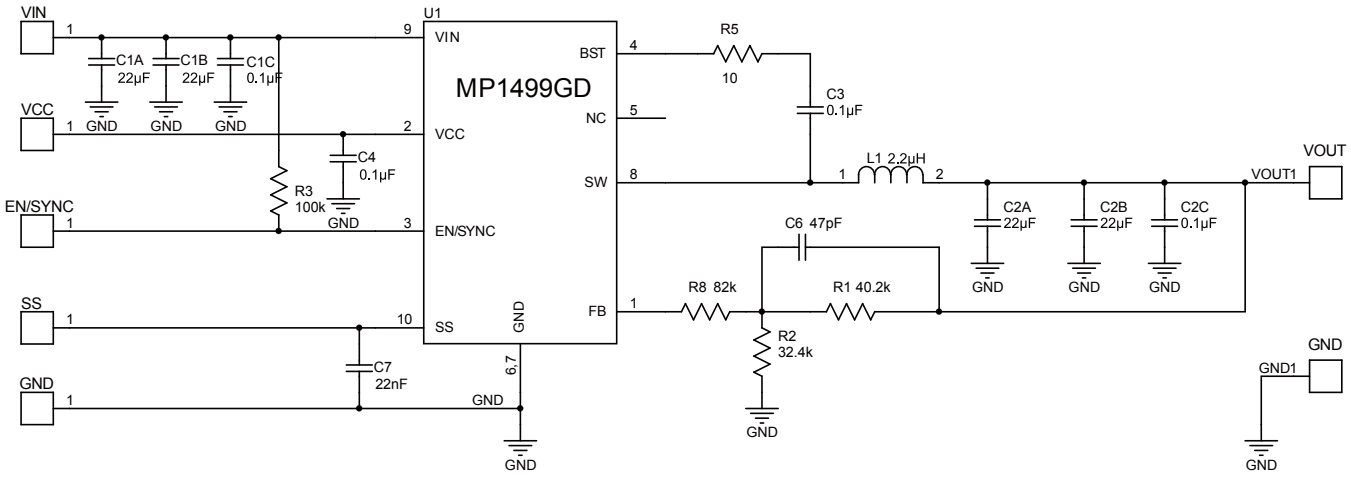


Figure 11—12V Input-1.8V/5A Peak Output

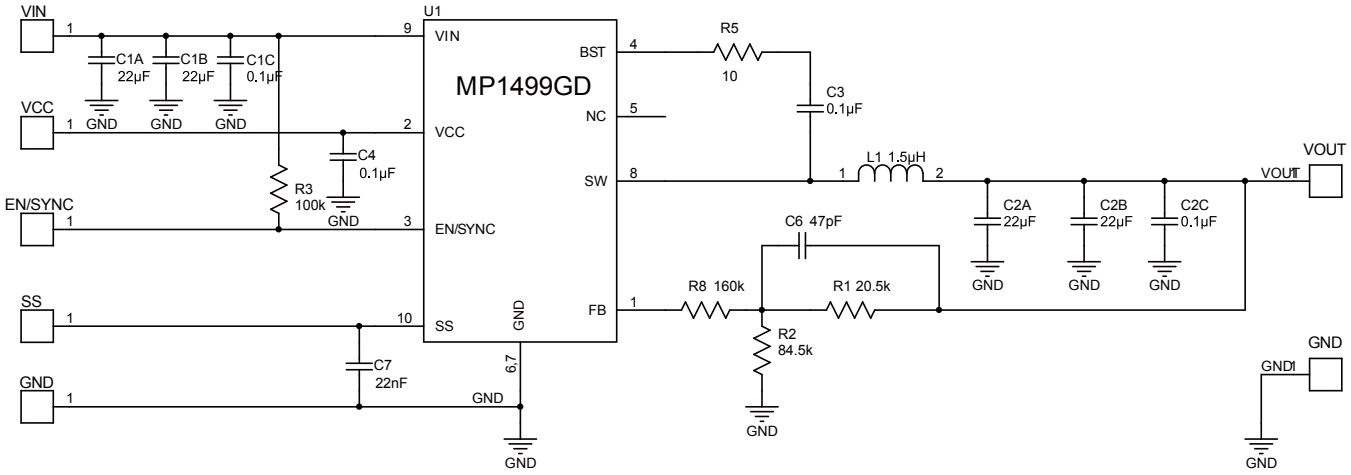
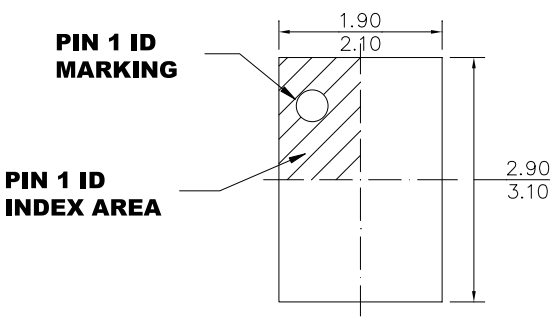


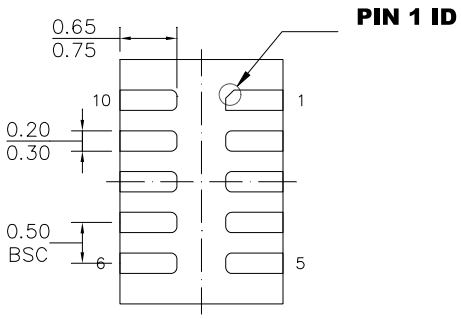
Figure 12—12V Input-1V/5A Peak Output

PACKAGE INFORMATION

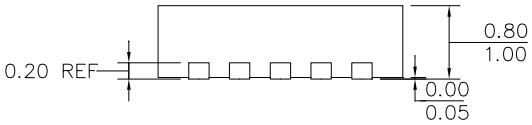
QFN10 (2X3mm)



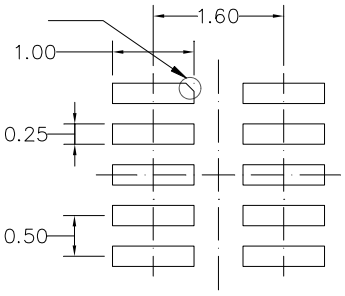
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.